1 TRANSMITTING TRANSISTOR DESIGN

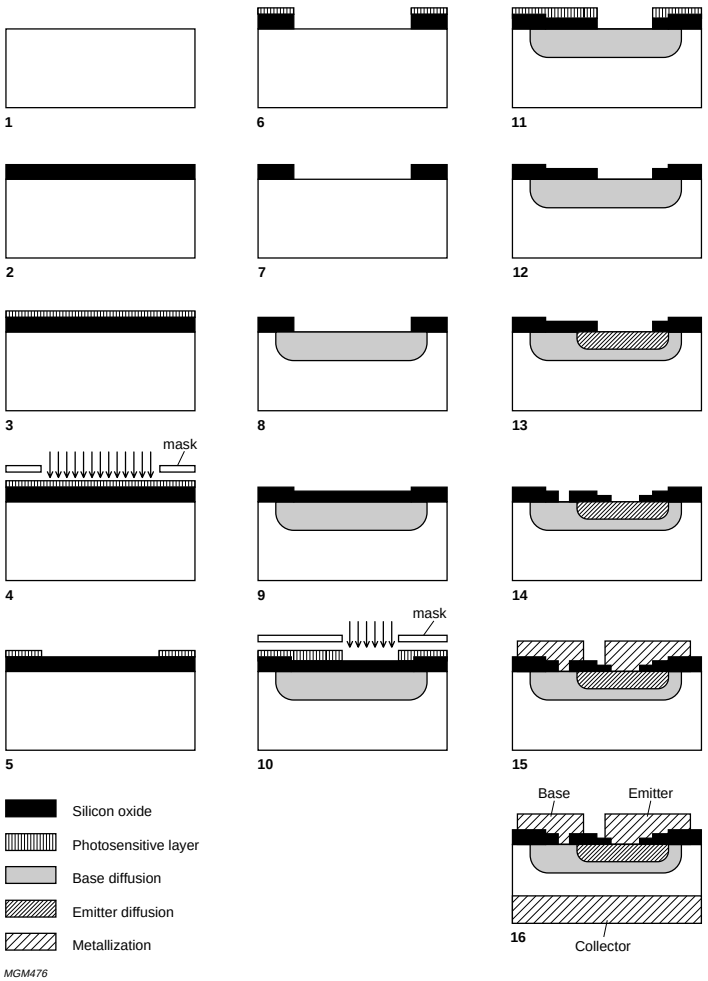
1.1 Die technology and design

A transmitting transistor has to deliver high power at high frequency (>1 MHz). This means that a large transistor die with a fine structure is required. Bipolar and MOS transistors are suitable, see panel, and Philips Semiconductors' portfolio includes both types. Their relative merits are summarized later in this section. First, however, let's look at the basic aspects of design that contribute to the reliability and high-performance of a modern RF transmitting transistor.

TRANSISTOR FABRICATION

As is well-known, most transistors are fabricated from silicon wafers (5" dia. or larger, and about 0.25 mm thick) in a multi-stage batch process that involves precise, localized doping of an epitaxial layer grown on the silicon substrate to form the different transistor regions. The main process steps for fabricating bipolar transistors are shown here as a reminder. MOS transistors are fabricated using similar techniques. Though semiconductor manufacturers have many processes available to meet different commercial and technical specifications, they all are based on the principles outlined below.

1. Silicon wafer
2. Oxidize to form oxide layer
3. Apply photosensitive layer
4. Expose through high-resolution mask
5. Develop photosensitive layer
6. Etch base window through oxide layer
7. Remove remaining photosensitive layer
8. Diffuse or ion-implant the base
9. Oxidize base window
10. Expose emitter window
11. Etch emitter window through oxide layer
12. Remove remaining photosensitive layer
13. Diffuse or ion-implant the emitter
14. Create metallization window
15. Metallize base and emitter regions
16. Polish and metallize bottom (collector).



1.1.1 Bipolar transistor dies

1.1.1.1 THE COLLECTOR (SUBSTRATE MATERIAL)

All of Philips' present bipolar types are NPN silicon planar epitaxial transistors, see Figs 1-1 and 1-2. The basic epitaxial material consists of a highly doped n-substrate (100 to 200 μm thick) with a rather high ohmic n-layer (epi-layer) deposited on top. The resistivity of this layer determines the collector-base breakdown voltage of the device ($V_{(BR)CBO}$). Most Philips transistors intended for operation at a supply voltage of 28 V have a *guaranteed* breakdown voltage of 65 V (and a typical value of about 80 V). The required resistivity of the epi-layer for this breakdown voltage is 1.6 to 2.0 Ωcm, the exact value having a very small tolerance.

A second important design parameter is the epi-layer thickness, which must be thicker than the collector depletion layer thickness at breakdown to prevent reverse second breakdown when the base current is negative. This occurs when the collector voltage is higher than the collector-emitter breakdown voltage with open base, $V_{(BR)CEO}$. Normally, this voltage is about half the collector-base breakdown voltage mentioned earlier. When the collector voltage is between these two collector breakdown voltages ($V_{(BR)CBO}$ and $V_{(BR)CEO}$), the situation is as shown in Fig.1-3.

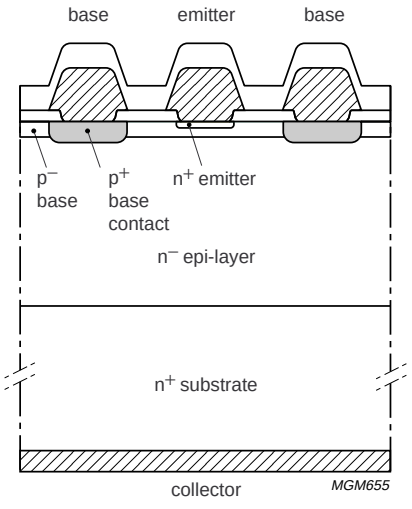


Fig.1-1 Cross-section of a bipolar transmitting transistor.

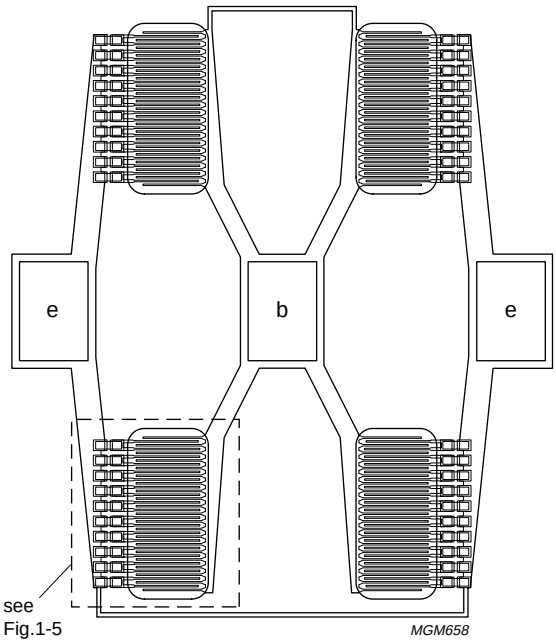


Fig.1-2 Layout of a typical bipolar transmitting transistor die.

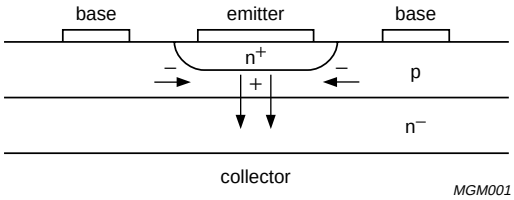


Fig.1-3 When the collector voltage is between $V_{(BR)CBO}$ and $V_{(BR)CEO}$, very high current densities are formed under the emitter. The arrows indicate the direction of electron current.

As Fig.1-3 shows, the collector current is concentrated in the middle of the emitter which can lead to very high current densities. The base is negative along the edge of the emitter and positive beneath it. If this situation continues for a long time, it will eventually destroy the transistor. This effect can be reduced by making the epi-layer somewhat thicker than strictly necessary, the chosen thickness being a compromise between the transistor's RF performance and its ability to withstand certain forms of output mismatching.

1.1.1.2 THE EMITTER AND BASE

The emitter of an RF power transistor must be dimensioned such that the transistor can deliver the required output power with all performance-degrading effects such as capacitances minimized. To achieve this, both the emitter area and periphery are important parameters, because of 'emitter-crowding', see Fig.1-4.

The base (electron) current makes the base positive along the edge of the emitter but negative in the middle. This means that collector current only flows at the edge of the emitter, so the potential output power is mainly determined by the emitter periphery. Under normal operating conditions, only 1 to 2 μm of the edge of the emitter is active; the rest of the emitter merely introduces parasitic capacitance. A practical choice for emitter width is 2 to 4 μm.

For a 2 to 4 μm wide emitter, a good design rule of thumb is that every watt of output power requires about 2 mm of emitter periphery. A narrower emitter can improve some characteristics, but requires more emitter periphery per watt.

Of course, it is not very practical to make one extremely long, narrow emitter, so transistor designers use an interdigitated structure as shown in Fig.1-5. In this structure, the emitter is split into several parallel parts ('fingers') with the base contacts in between. The finger pitch is mainly determined by the maximum frequency of operation - the higher the frequency, the smaller the pitch.

The emitter fingers are normally connected at one end by metallization. As a result, there is a voltage drop along each finger. This must not exceed 25 to 30 mV at maximum collector current otherwise part of the finger will be cut off near the other end.

Splitting the emitter into many sections is thus required for practical reasons and for good operation. This is also true to some extent for the base, but for different reasons. In fact, if the required output power is low, say 2 to 3 W, a single base area is acceptable. At higher powers, it is necessary to split the base area into several parts as this:

– Reduces the thermal resistance of the die
– Increases the base periphery, improving the distribution of dissipation at breakdown since collector breakdown occurs first along the edges of the base areas
– Allows more base and emitter bonding pads to be included, which reduces the emitter lead inductance, increasing the power gain. In addition, splitting the base area reduces the current through each bonding wire.

The preferred distance between successive base areas is approximately twice the die thickness, say about 300 μm, to obtain a low thermal resistance. A disadvantage of splitting the base is higher parasitic capacitances.

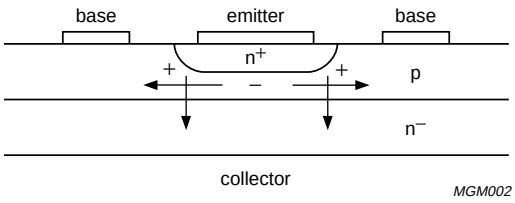


Fig.1-4 Emitter crowding effect. The arrows indicate the direction of electron current in normal operation. Note, to prevent confusion, the base current has also been drawn as an electron current.

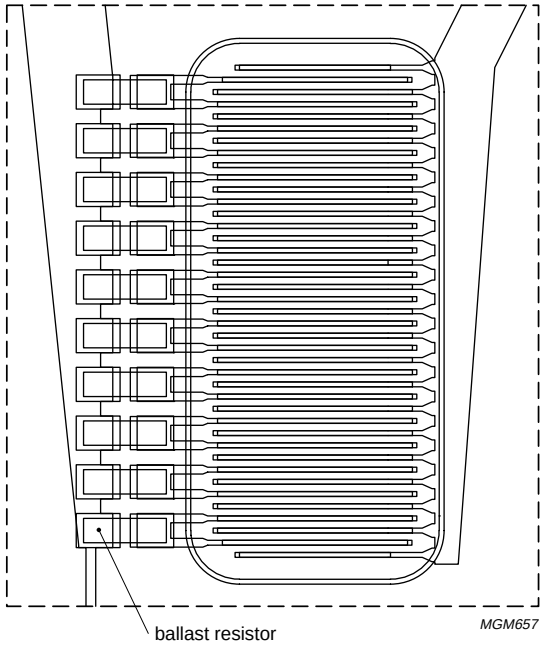


Fig.1-5 Interdigitated base-emitter structure.

1.1.1.3 EMITTER BALLAST RESISTORS

For electrical ruggedness, a built-in emitter ballast resistor is virtually a necessity. This is certainly the case when class-A or class-AB operation can be expected. In class-A for instance, without such an emitter resistor, the collector current can become restricted to a small area in the middle of the die where the temperature is highest. This causes a large increase in the thermal resistance which can destroy the transistor at a much-reduced DC power.

To prevent this effect, each emitter finger or group of two fingers, is provided with an emitter resistor. Good current distribution is obtained if the total emitter resistance is such that the voltage drop across it is approximately 200 to 300 mV at the normal DC collector current.

Emitter resistors can be made as a p^+-diffusion beside the base areas (Fig.1-6a) or as a doped polysilicon layer on top of the oxide (Fig.1-6b), the latter producing less parasitic capacitance.

The temperature coefficient (t.c.) of a diffused emitter resistance is positive, and at practical operating temperatures (~125 °C), the resistance increases by approximately 0.1%/K. The t.c. of a polysilicon resistor is much smaller.

1.1.1.4 DIFFUSION AND IMPLANTATION PROCESSES

The first transmitting transistors were made using diffusion processes. Nowadays, ion implantation followed by temperature treatment is the preferred manufacturing process as it provides superior reproducibility and sharper (i.e. better defined) doping transitions. The specific implantation process used depends primarily on the maximum frequency of operation required. For the highest frequency transistors, extremely shallow implantations are used, giving a thin base and a high f_T. The resulting h_{FE}, usually about 50, is ample for RF operation.

1.1.2 Vertical DMOS transistor dies

1.1.2.1 THE DRAIN (SUBSTRATE MATERIAL)

Philips' RF power MOS transistors are all silicon n-channel enhancement types, (see Fig.1-7). The considerations for and dimensioning of the epitaxial material are principally the same as those for bipolar transistors (Section 1.1.1.1).

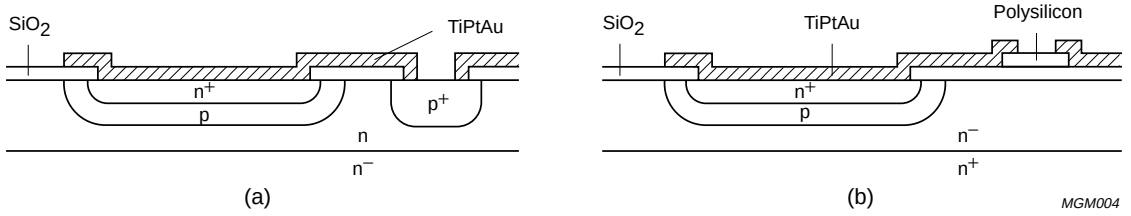


Fig.1-6 Emitter resistance formed (a) by a p^+-diffusion beside the base areas, and (b) as a doped polysilicon layer on top of the oxide.

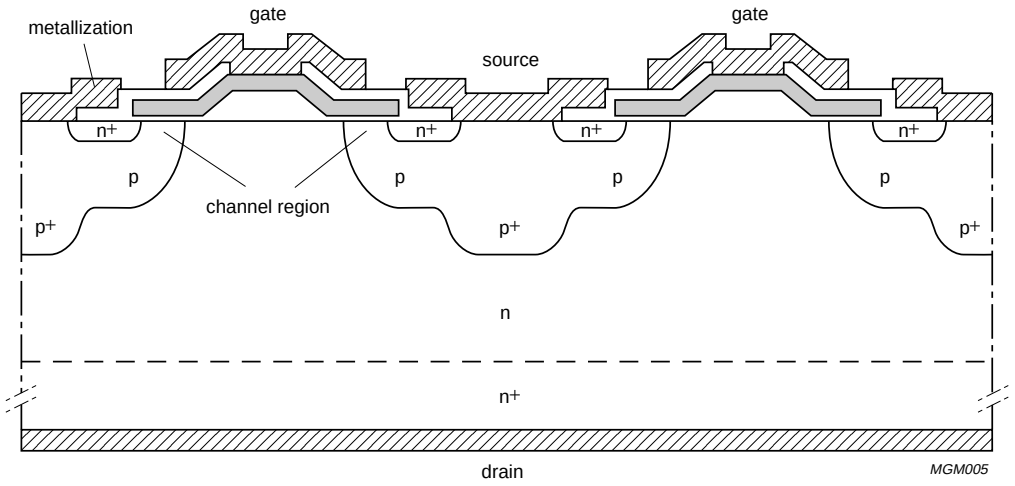


Fig.1-7 Cross-section of a vertical DMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.2.2 THE SOURCE AND GATE

The configuration of source and gate in most MOS transmitting transistors is similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-9.

The RF output power that such a device can deliver depends of course on the maximum drain current (I_{DSX}) which, in turn, is directly proportional to the width of the gate (approximately equal to the 'channel width'). To facilitate comparison with bipolar transistors, the source periphery (virtually the same as the total channel width) is used. Dimensioning is then very similar to that of a bipolar transistor, namely 2 to 3 mm of source periphery per watt of output power.

An equivalent to the emitter ballast resistors of a bipolar transistor is not required. This is because the temperature coefficient of the drain current as a function of the gate voltage is negative at high drain currents, providing automatic protection against thermal runaway, see Fig.1-8.

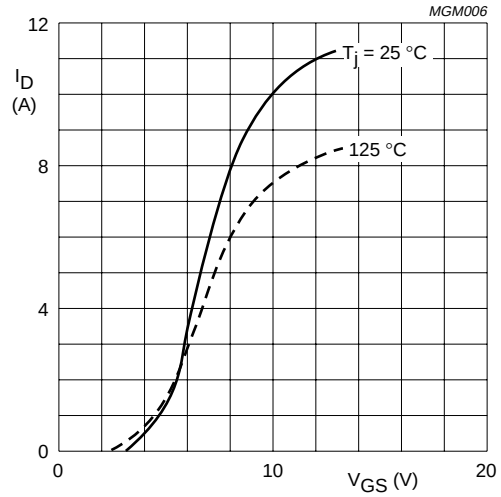


Fig.1-8 At high drain currents, the negative temperature coefficient of the drain current vs. gate voltage protects against thermal runaway.

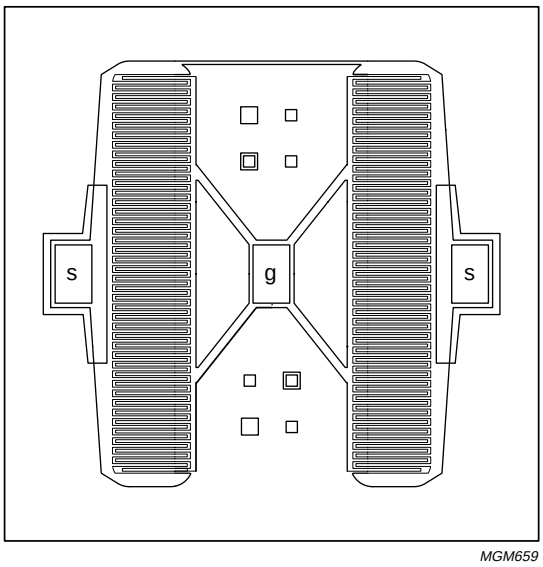


Fig.1-9 Interdigitated source and gate arrangement of a typical MOS transmitting transistor die. Die size: 1×1 mm^2.

1.1.2.3 THE CHANNEL REGION

As for bipolar devices, the process used to manufacture a MOS transistor is dependent on the intended maximum operating frequency. A key parameter is the length of the channel, l_{ch}, (gate) because it determines the cut-off frequency, f_T:

$$f_T = \frac{G_{fs}}{2\pi C_{is}} = \frac{V_{sat}}{4\pi l_{ch}}$$

where:

G_{fs} is the forward transconductance

C_{is} is the input capacitance

V_{sat} is the saturation velocity (for silicon: 10^7 cm/s)

and

l_{ch} is the channel (gate) length.

1.1.2.4 COMPARISON OF VDMOS AND BIPOLAR TRANSISTORS

Both Philips' bipolar and MOS types can provide excellent performance. At high frequencies (~1 GHz and above), bipolar transistors usually provide the best all-round performance. At lower frequencies, VDMOS devices can outperform bipolar types, e.g. on power gain, and will likely capture an increasing part of the present bipolar market as performance continues to improve.

Table 1-1 VDMOS and bipolar devices compared

ADVANTAGES OF VDMOS	DISADVANTAGES OF VDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents.	**The gate is sensitive to electrostatic charges** so ESD protection measures must be taken.
Lower noise. This is especially important in duplex equipment and where many transceivers are operating near to each other and at similar frequencies.In one test, an improvement of 7 dB was measured at 75 MHz in similar wideband amplifiers.	**Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.
Higher power gain (up to ~5 dB higher) than comparable bipolar types at lower frequencies. This is mainly due to the high transconductance and low feedback capacitance.	
Simple control of the output power. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage.	
Superior thermal stability owing to the negative temperature coefficient of the drain current at high levels, this is also why the current distribution over the whole active area of a VDMOS device is so good.	
Superior load mismatch tolerance - Another benefit of the superior thermal stability of a VDMOSFET.	
Lower high-order (7th and higher) intermodulation products due to the 'smoother' characteristics of MOS devices.	

1.1.3 Lateral DMOS (LDMOS) transistor dies

LDMOS technology is a relatively recent development. Unlike VDMOS which can be used up to about 1 GHz, LDMOS, like bipolar, is suitable for use at higher frequencies owing to its lower feedback capacitance and source inductance than VDMOS. However, depending on the particular performance and cost requirements, VDMOS, LDMOS or bipolar can provide the best solution.

1.1.3.1 THE SOURCE (SUBSTRATE MATERIAL)

Philips LDMOS transistors are all silicon n-channel enhancement types, (see Fig.1-11). The substrate is highly doped p-material, whereas the epitaxial layer is lightly doped p^--material.

1.1.3.2 THE DRAIN AND GATE

The configuration of drain and gate is fairly similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-10. Note however that *all regions, (gate, source and drain) are metallized on top of the die*. The gate and drain are connected to bonding pads, and the source is grounded to the substrate by means of a via-diffusion through the epi-layer. The benefit of this design is that a *single* metal interconnect can be used. Note, the top source metallization is solely for interconnecting the p^+ and n^+ regions; the transistor's source electrode is connected to the bottom (substrate) metallization.

As for a VDMOS device, the RF output power that an LDMOS device can deliver depends on the maximum drain current (I_{DSX}) which is directly proportional to the width of the gate (approximately equal to the 'channel width'). And, an equivalent to the emitter ballast resistors of a bipolar transistor is again not required, see Section 1.1.2.2.

1.1.3.3 THE CHANNEL REGION

As with VDMOS, a key parameter of an LDMOS transistor is the length of the channel, l_{ch} (gate) because it determines the cut-off frequency, f_T (defined as for VDMOS in Section 1.1.2.3).

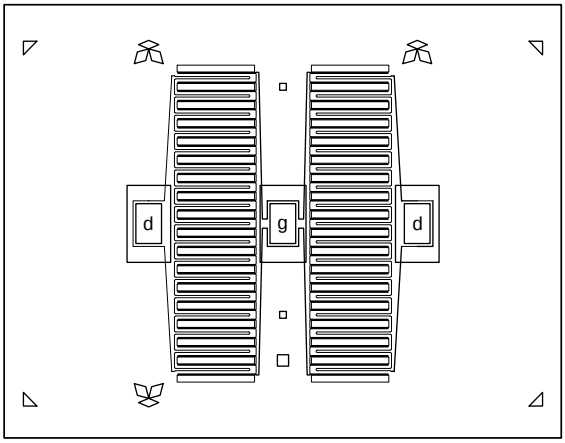


Fig.1-10 Interdigitated drain, source and gate arrangement of a typical LDMOS transmitting transistor die.
Die size: 1×0.8 mm^2.

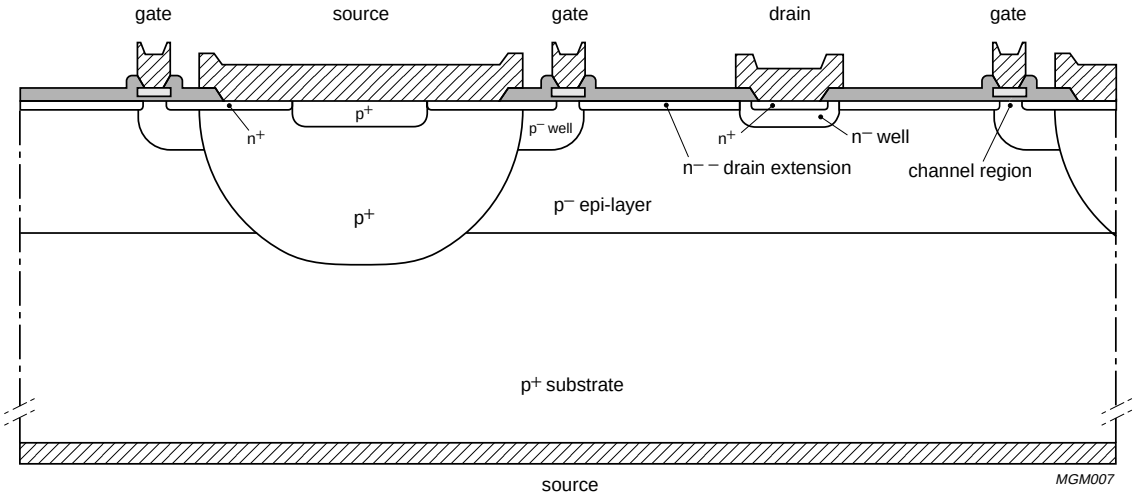


Fig.1-11 Cross-section of an LDMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.3.4 COMPARISON OF LDMOS AND BIPOLAR TRANSISTORS

Both Philips' LDMOS and bipolar transistors can provide excellent performance in a variety of applications. Nevertheless, there are some differences. For example, the lateral structure of an LDMOS transistor means it has a very low feedback capacitance compared with a bipolar transistor. And as power gain is directly related to the feedback capacitance and source (or emitter) inductance, this means an LDMOS transistor has higher power gain. Furthermore, an LDMOS transistor has superior intermodulation distortion performance over a large dynamic range.

Table 1-2 LDMOS and bipolar devices compared

ADVANTAGES OF LDMOS	DISADVANTAGES OF LDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents. **Higher power gain** than comparable bipolar types. This is due to the low source inductance and low feedback capacitance. **Simple control of the output power**. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage. **Superior thermal stability** owing to the negative temperature coefficient of the drain current at high levels. This is also why the current distribution over the whole active area of an LDMOS device is so good. **Superior load mismatch tolerance** - another benefit of the superior thermal stability of an LDMOSFET. **Lower high-order (7th and higher) intermodulation products** due to the 'smoother' characteristics of MOS devices.	**The gate is sensitive to electrostatic charges**, so ESD protection measures must be taken. **Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.

1.2 Transistor equivalent circuit

At this point, it is useful to introduce a basic equivalent circuit of a bipolar RF transmitting transistor, and a few simple expressions that indicate the behaviour of power gain, input and load impedance under different conditions. This will assist the understanding of the following section on internal matching.

Figure 1-12 shows a simple equivalent circuit of an RF transistor with load circuit. Note, the emitter inductance, L_E, affects transistor performance significantly as we shall see presently.

1.2.1 Main elements

The collector-to-base feedback capacitance consists of two parts (see Fig.1-1, transistor cross-section):

– *An intrinsic part C_{BCi}:* the capacitance of the reverse biased collector-to-base junction in the regions below the emitter

– *An extrinsic part C_{BCe}:* the capacitance of the same junction beyond the emitter. C_{BCe} also includes parasitic capacitances introduced by the base metallization.

The sum of these capacitances, C_{BCt}, is published in data sheets as C_{re}:

$$C_{re} = C_{BCi} + C_{BCe}$$

R_B represents the series resistance of the base layer, and R_E is the emitter ballast resistance. C_{BE} represents the total forward biased base-emitter capacitance which is mainly determined by the diffusion capacitance, and which varies directly with the emitter current. This capacitance is normally shunted by a resistor, omitted here, since at high frequency operation, virtually all current flows into C_{BE}.

The collector is terminated by a load resistance R_L shunted by an inductance L_L which resonates with the total collector-to-base capacitance. Approximate expressions for these circuit elements are:

$$L_L = \frac{1}{\omega^2 C_{BC}} \text{ and } R_L = \frac{V_C^2}{2P_L}$$

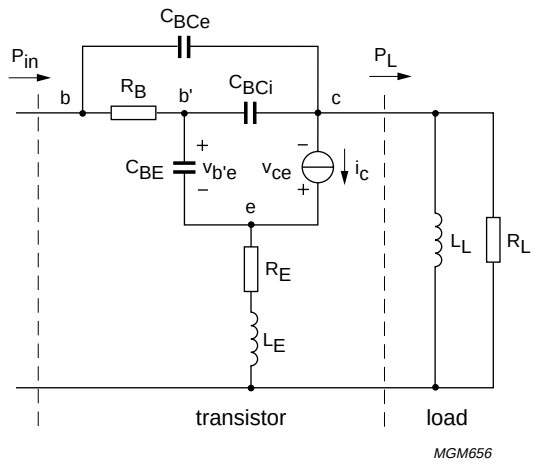
At high frequencies, the collector current, i_c, is proportional to the base-emitter current, i_{be}, and lags the latter by 90°:

$$i_c \approx i_{b'e}\left(\frac{\omega_T}{j\omega}\right)$$

Clearly, the high frequency common-emitter current gain, h_{fe}, is approximately ω_T/ω.

To simplify the following approximations, it has been assumed that:

– For maximum power, the collector circuit is in resonance, i.e. v_{ce} and i_c are in antiphase
– The base potential is very small compared to the collector voltage
– All collector parasitics are part of the load circuit.



b: Base.
c: Collector.
e: Emitter.

Fig.1-12 Simple equivalent circuit of a bipolar RF transmitting transistor.

1.2.2 Input impedance

With these assumptions, the input impedance, Z_{in}, can be approximated by:

$$Z_{in} = \left[\frac{1}{1+\omega_T C_{BCt} R_L}\right] \times$$

$$\left[(1+\omega_T C_{BCi} R_L)\, R_B + \omega_T L_E + R_E + j\omega L_E + \frac{1}{j\omega}\left(\frac{1}{C_{BE}} + R_E \omega_T\right)\right]$$

Note that emitter inductance effectively increases the total input resistance by $\omega_T L_E$. The emitter ballast resistance R_E appears as a series capacitance $1/R_E\omega_T$, decreasing the total input capacitance. Based on this expression, the total input impedance can be represented by a series RLC equivalent circuit, see Section 1.3.1.

1.2.3 Power gain

The power gain, Gp, can be approximated by:

$$G_p = \frac{P_L}{P_{in}} = \left(\frac{\omega_T}{\omega}\right)^2 \left(\frac{1}{1+\omega_T C_{BCt} R_L}\right) \times \left(\frac{R_L}{(1+\omega_T C_{BCi} R_L)\, R_B + R_E + \omega_T L_E}\right)$$

Note that emitter inductance L_E reduces power gain and is a key performance-determining factor in high-frequency transistors. It depends on bonding wire and package inductances. Other important parameters affecting power gain are R_E and these are determined by the active parts of the die design.

1.2.4 Large-signal expressions

The expressions given for Z_{in} and G_p relate to class-A amplifiers operating in the linear (i.e. small-signal) region. For large-signal operation, several elements become non-linear. The expressions can however still be used for a first-order approximation by substituting *average* values for the voltage and current dependent elements. In addition for class-B and class-C operation, the conduction angle, which affects the average value of ω_T, should be taken into account.

1.3 Internal matching

Impedance matching is required to optimize the performance of a transmitting transistor in the application for which it was designed. Internal matching raises impedances and improves wideband capability. To assist designers, many of Philips' transmitting transistors already incorporate internal matching circuitry, simplifying or reducing the external matching required.

1.3.1 Input matching

Figure 1-13 shows the equivalent circuit of the input impedance of a bipolar transmitting transistor without matching circuitry.

At high frequencies, the capacitor has very low reactance and can be neglected in most cases. In a high-power transistor, the resistor becomes very small, typically <1 Ω, as such a device can be considered as many small 'transistors' in parallel The inductor, which is normally 1 to 2 nH, has a rather high reactance in the UHF region, so the input Q becomes high, making wideband matching difficult if not impossible, while circuit losses increase significantly. To compensate for these effects, an additional capacitor is often fabricated 'inside' the transistor such that the transistor equivalent circuit is as shown in Fig.1-14.

This capacitor, together with the base and emitter inductances, forms a first matching section that raises the input impedance to a more acceptable level. The resonant frequency of the section is set to be somewhat above the maximum operating frequency for which the transistor is intended.

An additional advantage of this configuration is that it increases the power gain slightly at the high end of the frequency band, not only because of reduced circuit losses, but mainly because the capacitor is, in effect, connected to a tap on the emitter lead inductance, overcoming a major cause of reduced power gain at high frequencies (emitter lead inductance).

A MOS capacitor is used, and it can only be used in transistor packages with two emitter 'bridges': one, the normal elevated bridge; the other, an integrated bridge on the beryllia disc to which the capacitor is soldered. The maximum performance improvement is obtained with packages having *four* emitter connections (see Fig.1-15). Better still of course are packages with internal emitter grounding.

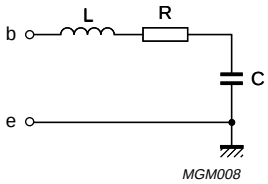


Fig.1-13 Equivalent circuit of the input impedance of a bipolar transmitting transistor. For high-frequency high-power operation, matching circuitry is required. b: base; e: emitter.

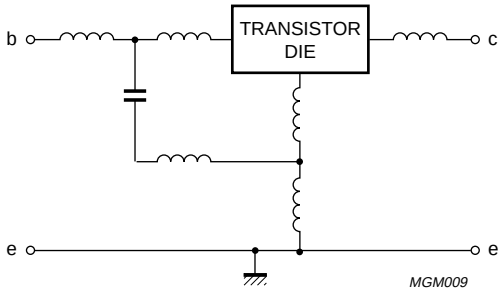


Fig.1-14 Equivalent circuit of a bipolar transmitting transistor with internal input matching. Adding an internal capacitor improves wideband matching.

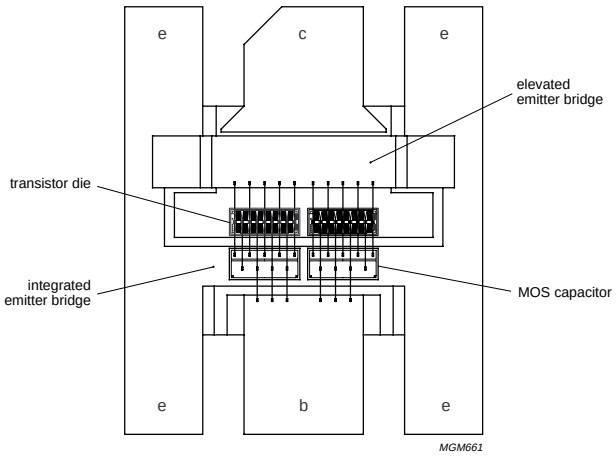


Fig.1-15 Position of the MOS input matching capacitor in a package with two emitter bridges, and four emitter connections.

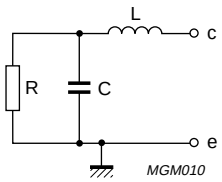


Fig.1-16 Large-signal equivalent circuit of the output of an RF power transistor.
L: collector and emitter lead inductance;
C: effective output capacitance;
R: optimum load resistance. Note, R is the load resistance that produces maximum output. It is not a physical resistor in a transistor and its value varies according to the application.

1.3.2 Output matching

At the output of a transistor, the situation is somewhat different, see Fig.1-16.

In wideband matching circuits, it is desirable to tune out (with inductive shunt) the capacitor C somewhere in the frequency band for which the transistor is intended. In practice, the best results are obtained when the resonant frequency is in the lower part of the band.

If an *external* shunt inductor were used for this purpose, the result would be a very low inductive tap, making further matching extremely difficult, especially at high powers and frequencies. A better solution would be to tune out the collector capacitance *inside the transistor package*. This is done in practice in balanced (push-pull) transistors by adding a metallized strip onto the beryllia or aluminium nitride disc. In single-ended devices, it is done by connecting one side (the other is grounded) of a MOS capacitor that provides isolation to the collector via bonding wires that form the required shunt inductance, see Fig.1-17.

A disadvantage of this approach in both cases is that such a transistor is unsuitable for use in frequency bands lower than the one for which it is intended. This limitation is outweighed however by the higher load impedance and lower Q-factor, resulting in lower losses in the matching circuit and improved wideband performance.

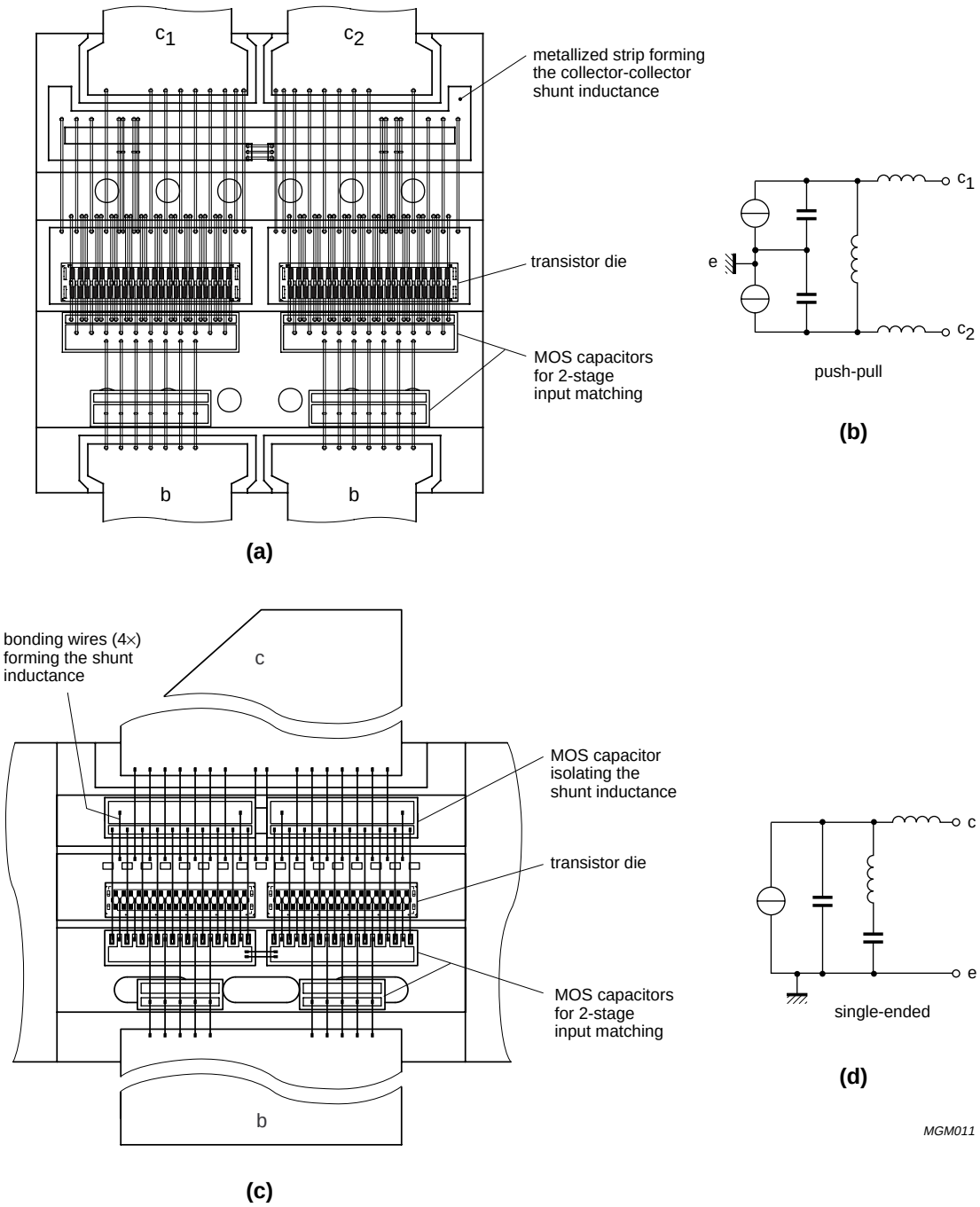


Fig.1-17 Bonding arrangement of (a) a BLV861 intended for use in push-pull configuration (b), and (c) bonding arrangement of a BLV2045 intended for single-ended configuration (d).

2 RF POWER TRANSISTOR CHARACTERISTICS

This section describes how to interpret and use the data published by Philips Semiconductors on its transmitting transistors.

2.1 Bipolar devices

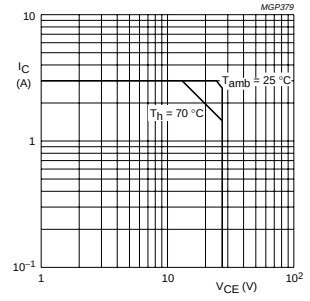
2.1.1 Limiting values (Ratings)

As an example, consider the published data (Fig. 2-1) for the BLV59, a 30 W transistor intended for operation at up to 860 MHz from a supply voltage of 25 V, and used mainly in class-AB linear operation in TV transmitters.

LIMITING VALUES

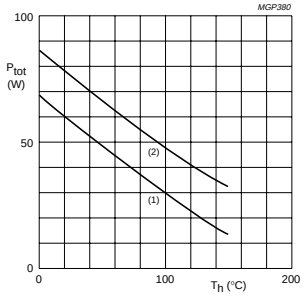
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
I_{CM}	peak collector current	f > 1 MHz	–	9	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; f > 1 MHz	–	70	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C



$R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.2 DC SOAR.



(1) Continuous operation (f > 1 MHz).
(2) Short-time operation during mismatch (f > 1 MHz).

Fig.3 Power/temperature derating curves.

Fig.2-1 Part of the BLV59 data sheet showing how device *ratings* are specified.

2.1.1.1 DEFINITIONS

V_{CBO} *The maximum collector-base voltage with open emitter,* which must never be exceeded in normal operation. If this voltage is exceeded slightly, the transistor will probably not be damaged immediately. However, it will certainly produce a lot of wideband noise if the peaks of the RF voltage reach the avalanche breakdown voltage.

For some transistors, V_{CES}, the maximum collector-emitter voltage with a short circuit between base and emitter is specified. V_{CES} is almost equal to V_{CBO}.

V_{CEO} *The maximum collector-emitter voltage with open base.* The supply voltage must always be lower than this voltage otherwise the base current becomes negative. And, as there is always some DC resistance between base and emitter, this can lead to reverse second breakdown.

For some transistors, V_{CER}, the maximum collector-emitter voltage with a small resistor e.g. 10 Ω, between base and emitter is specified. V_{CER} is slightly lower than V_{CBO} and V_{CES}. With higher resistances, this voltage can approach V_{CEO}.

The relation between the different collector breakdown voltages is illustrated in Fig.2-2.

V_{EBO} *The maximum emitter-base voltage with open collector.* When the transistor is used in class-C, the average base-emitter voltage is negative, and V_{EBO} can easily be exceeded. Life tests performed under such conditions have shown that parameters such as h_{FE} and leakage currents can deteriorate. Philips Semiconductors therefore does not advise class-C operation of bipolar transistors except when the negative base-emitter bias voltage is a few tenths of a volt.

I_C *The maximum collector DC current.* This is specified to protect the emitter bonding wires and the die metallization.

I_{CM} *The maximum instantaneous value of the collector current.* Characteristics such as h_{FE} and f_T deteriorate rapidly above this value, making operation at higher levels impractical.

P_{tot} *The maximum RF dissipation at a mounting base temperature of 25 °C.* This is given only to enable different devices to be compared. In practice, the mounting base temperature will always be higher than 25 °C.

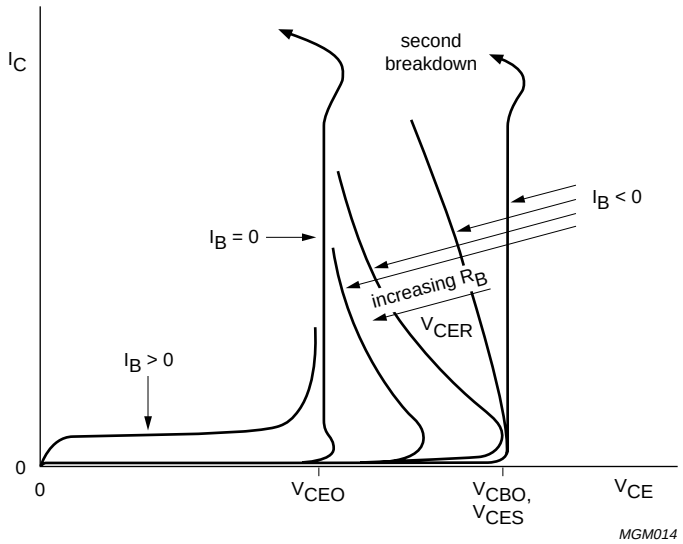


Fig.2-2 Definition of breakdown voltages.

T_{stg} *The maximum ($T_{stg\ max}$) and minimum ($T_{stg\ min}$) temperatures at which a device may be stored when not in operation.* These limits maximize storage life.

T_j *The maximum junction temperature in operation.* This is 200 °C for most silicon devices. Exceeding this value for long periods will shorten transistor life.

DC SOAR

The DC Safe Operating ARea.
This is a graph showing the maximum allowable DC collector current versus the collector-emitter DC voltage at a specified mounting base (and/or heatsink) temperature. This information is essential if a device is used in class-A. Note that the thermal resistance in DC operation is often higher (i.e. worse) than the resistance in RF operation. However, for a well-designed device, i.e. one with a built-in emitter resistance of sufficiently high value, the differences between the DC and RF SOAR are small.

Some transistors designed specifically for class-B operation have smaller built-in emitter resistances, so the allowable DC dissipation at high collector voltages is reduced to prevent forward second breakdown at these voltages. Figure 2-3 gives an example of such a DC SOAR.

Power/temperature derating curves versus heatsink temperature.
These curves give the maximum allowable RF dissipation under different conditions. A transistor's thermal resistance is not constant because the thermal resistivities of silicon, beryllia and aluminium nitride are temperature dependent, all increasing with temperature. Therefore, the thermal resistance of the transistor depends on the heatsink or mounting-base temperature and on the power dissipation.

The curve given for continuous operation (Curve I) is based on a junction temperature of 200 °C. The other curve (Curve II) is for short-term operation under mismatch conditions and is based on a maximum junction temperature of 270 to 280 °C. Clearly, the latter sort of operation reduces transistor life and should be restricted as much as possible.

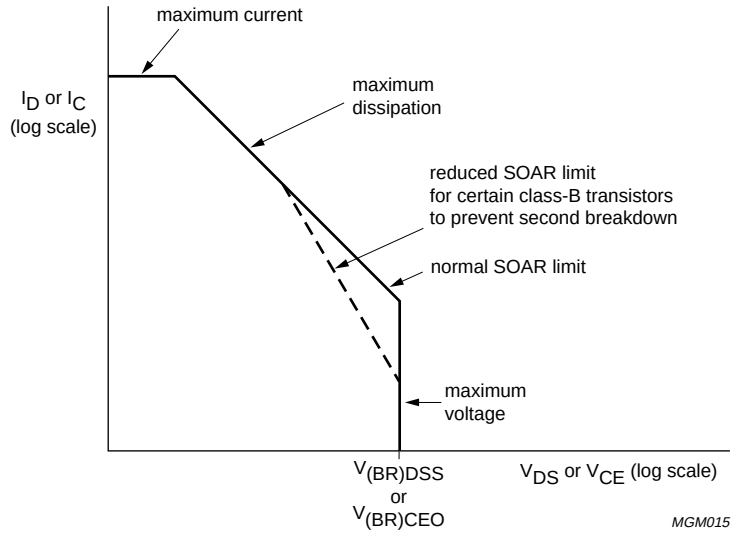


Fig.2-3 Example of a DC SOAR graph for a transistor designed specifically for class-B operation.

2.1.2 Characteristics

The BLV59 data sheet will again be used to illustrate how the main characteristics are presented in (see Fig.2-4)

2.1.2.1 THERMAL CHARACTERISTICS

Two thermal resistance values are given: from junction to mounting base, and from mounting base to heatsink. The former value is obtained from a well-defined, reproducible measurement taken under specified conditions and is guaranteed.

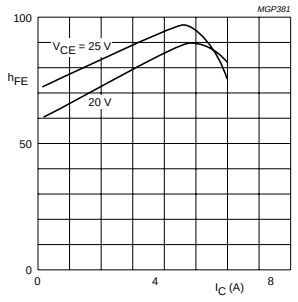
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C, P_{tot} = 50 W	2.3	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

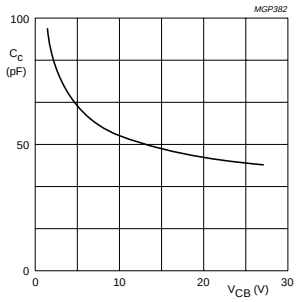
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 50 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector leakage current	V_{CE} = 27 V; V_{BE} = 0	–	–	10	mA
$E_{(SBR)}$	second breakdown energy	L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	4	–	–	mJ
h_{FE}	DC current gain	V_{CE} = 24 V; I_C = 2 A	15	–	–	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	44	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	30	–	pF
C_{cf}	collector-flange capacitance		–	2	–	pF



T_j = 25 °C.

Fig.4 DC current gain as a function of collector current; typical values.



$I_E = i_e$ = 0; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values

Fig.2-4 Part of the BLV59 data sheet showing how device *characteristics* are specified.

2.1.2.2 OTHER CHARACTERISTICS

Every transistor is subjected to a series of DC measurements to guarantee performance to specification. These measurements include the breakdown voltages mentioned earlier which are tested at specified currents, and the collector leakage current, in this example, I_{CES}, specified at a collector voltage of about half the breakdown voltage. Sometimes, other leakage currents such as I_{CEO} and I_{EBO} are specified.

h_{FE} *The DC current gain*
This is the ratio of collector and base current at specified V_{CE} and I_C. A minimum value is always given; a maximum
sometimes. Matched pairs of some transistor types are available for push-pull operation.

$E_{(SBR)}$ *The (reverse) second breakdown energy*
This is measured with a coil of 25 mH in the collector lead of the transistor. First, the collector current is adjusted such that:

$$I_C = \sqrt{\frac{2E_{(SBR)}}{L}}$$

where $E_{(SBR)}$ is the specified second breakdown energy.

The current is then suddenly interrupted, causing the collector voltage to rise to the avalanche voltage and to stay there
until all the energy of the coil ($LI_C{}^2/_2$) is dissipated by the transistor. If the collector voltage falls before a pre-set time that represents ideal transistor behaviour, the device is deemed unable to withstand the specified energy and fails the test.

A transistor's performance in the $E_{(SBR)}$ test gives a good indication of its RF mismatch performance. Moreover, since this test can be performed much quicker than a mismatch test and has no effect on transistor life, 100% testing of $E_{(SBR)}$ is used in production instead of mismatch-testing. Samples from production are of course subjected to real mismatch testing (see Section 2.1.3.3, Ruggedness) to establish quality levels.

Several other characteristics (typical values) such as capacitances and sometimes f_T and $V_{CE\,sat}$ are given:

C_c *The total collector or output capacitance.* This is the sum of C_{cb} and C_{ce} measured at 1 MHz.

C_{re} *The feedback capacitance, i.e. C_{cb}, also measured at 1 MHz.* Both capacitances are measured at the standard
supply voltage for each transistor type.

f_T *The transition frequency.* This is the frequency at which the RF value of the common-emitter current gain, h_{fe}, has fallen to one, see Fig.2-5, and is a useful performance indicator when comparing transistors. It is obtained in one measurement taken with the transistor output short-circuited. Above a certain frequency, the RF current gain, h_{fe} begins to fall off at 6 dB/octave. The measuring frequency, f_m, is chosen well above this frequency and then:
$f_T = h_{fe}f_m$.

Note: no f_T information is published for the BLV59, because this transistor has a built-in matching capacitor at its input
which would make the measurement meaningless.

$V_{CE\,sat}$ *The collector-emitter saturation voltage* gives an impression of the total resistance in the collector-emitter circuit. It is measured at an I_C/I_B ratio less than the specified minimum h_{FE} to ensure the transistor is saturated.

Finally, some graphs such as h_{FE} versus I_C, C_c versus V_{CB}, and in some cases f_T versus I_C are given.

All characteristics are published at T_j = 25 °C and (with the exception of the capacitances) are obtained from pulsed measurements using pulses of short duration compared to the thermal time constant of the die.

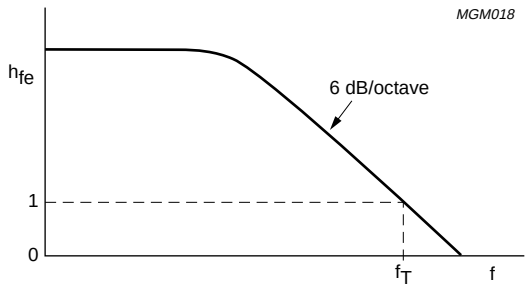


Fig.2-5 RF current gain, h_{fe} as a function of frequency. f_T is the transition frequency.

2.1.3 Application information

For each transistor type, a narrow-band test circuit is designed for the highest frequency of operation. The circuit is aligned for maximum power transfer and minimum input reflection. Important parameters such as power gain and collector efficiency (see Sections 2.1.3.1 and 2.1.3.2) are measured for each transistor from production.

To assist circuit designers, Philips Semiconductors publishes the circuit diagram and board lay-out of these test circuits (and the measured performance) in its data sheets, see Figs 2-6 and 2-7.

APPLICATION INFORMATION

RF performance up to T_h = 25 °C in a common emitter class-AB circuit; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

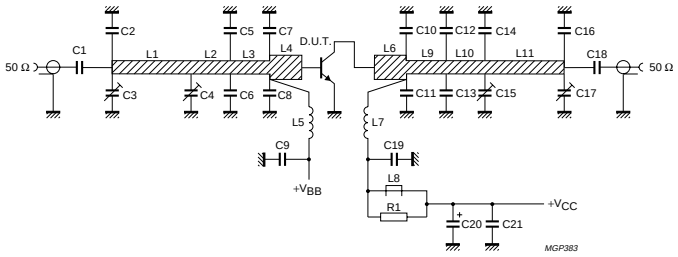
MODE OF OPERATION	f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	G_p (dB)	P_L (W)	η_C (%)	ΔG_p (dB)(1)
CW, class-AB	860	25	60	>7 typ. 8.5	30	>50 typ. 55	<1 typ. 0.2

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

Ruggedness in class-AB operation

The BLV59 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases at rated load power under the following conditions: V_{CE} = 25 V; f = 860 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA.



Temperature compensated bias (R_i < 0.1 Ω).

Fig.6 Class-AB test circuit at 860 MHz.

Fig.2-6 Part of the BLV59 data sheet showing the Class-AB test circuit for the BLV59 at f = 860 MHz. Fig.2-7 shows the board and component layout.
Though omitted here, component values, descriptions and manufacturers as well as board specifications and assembly instructions are given in the data sheets for each test circuit.

2.1.3.1 POWER GAIN

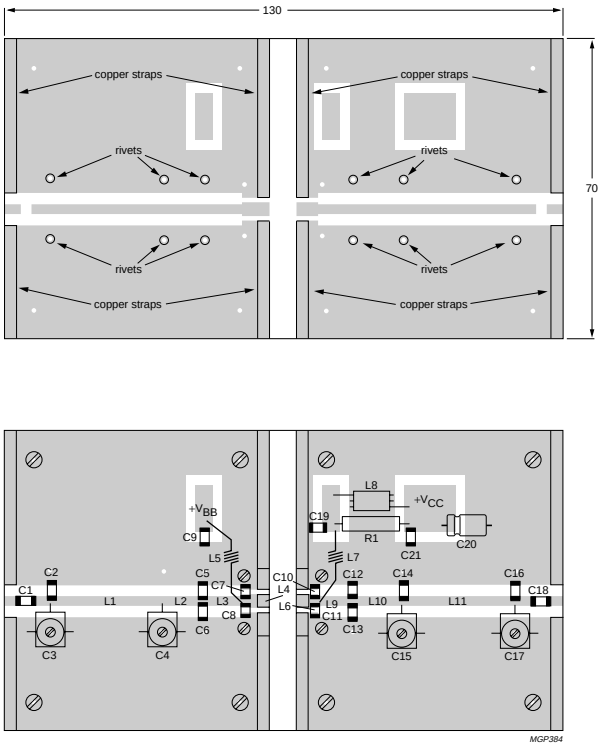
The power gain is defined as:

$$G_P = 10 \log\left(\frac{P_L}{P_S}\right) \text{ dB}$$

where:

P_L is the output power in the 50 Ω load

P_S is the forward power delivered by the 50 Ω source.



Dimensions in mm.

The components are situated on one side of the copper-clad PTFE-glass board, the other side is unetched and serves as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

Fig.7 Printed-circuit board and component layout for 860 MHz class-AB test circuit.

Fig.2-7 Board and component layout of the circuit shown in Fig.2-6.

2.1.3.2 COLLECTOR EFFICIENCY

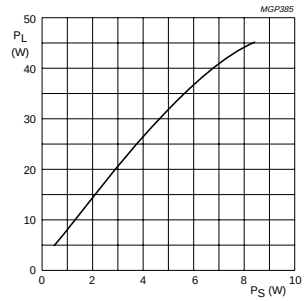
The collector efficiency is defined as:

$$\eta_c = \frac{P_L}{V_{CE} I_C} \times 100\%$$

where V_{CE} and I_C are the collector-emitter DC voltage and collector DC current respectively.

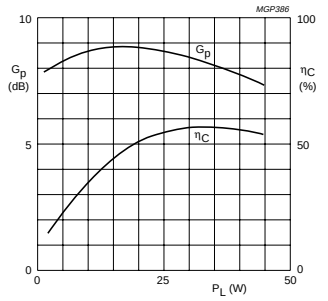
For the BLV59, the gain compression at maximum power (30 W) is also measured. The published values (all types) are all guaranteed.

Graphs are always given of load power versus source power and of power gain and efficiency versus load power (all typical values), see Fig.2-8.



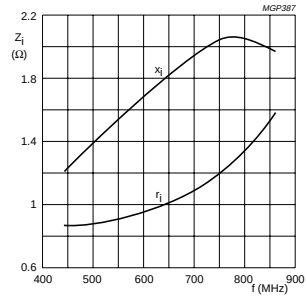
V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.8 Load power as a function of source power; typical values.



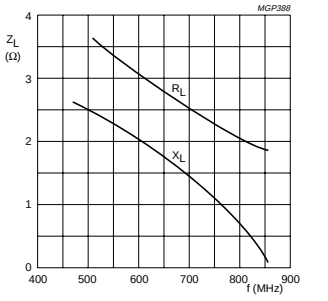
V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.9 Power gain and efficiency as a function of load power; typical values.



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.10 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.11 Load impedance as a function of frequency (series components); typical values.

Fig.2-8 Part of the BLV59 data sheet showing the performance (Figs.8 and 9) measured in the test circuit at a specified frequency (here 860 MHz).

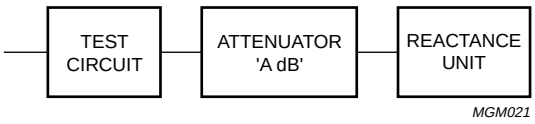


Fig.2-9 Circuit for measuring load mismatch tolerance.

2.1.3.3 RUGGEDNESS

Transistors are also tested for their ability to withstand output mismatching without any measurable degradation of performance (ruggedness). This is done by replacing the 50 Ω load impedance of the test circuit by an attenuator and reactance unit as shown in Fig.2-9.

The attenuator is dimensioned such that the VSWR required by the test is obtained according to:

$$A = 10 \log \left(\frac{s+1}{s-1} \right) \text{ dB}$$

where A is the attenuation and s is the VSWR.

The reactance unit is required to vary the phase of the reflection coefficient and has to be able to provide reactances from –∞ to +∞, including zero at the test frequency (usually the transistors maximum intended operating frequency). At very high frequencies, this can be done by means of a variable-length coaxial stub, variable over at least half a wavelength. At low frequencies, an LC circuit as shown in Fig.2-10 is used.

In this circuit, inductors L_1 and L_2 must be screened from each other. C_1 and C_2 is a ganged capacitor, and $C_1 = C_2$. Suitable component values are:

$X_{L1} = +j50\ \Omega$; $X_{L2} = +j200\ \Omega$

$X_{C1} = X_{C2} = -j200\ \Omega$ to $-j50\ \Omega$.

If C_1 and C_2 are set to their minimum value, the first series resonance (of L_2 and C_2) occurs, see Fig.2-11.

By increasing the capacitance of C_1 and C_2, the reactance can be varied from zero to +∞ at which a parallel resonance occurs. Increasing the capacitances further changes the reactance from –∞ to zero at which the second series resonance (of L_1 and C_1) occurs.

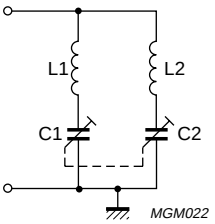


Fig.2-10 LC reactance circuit for mismatch measurements at low frequencies.

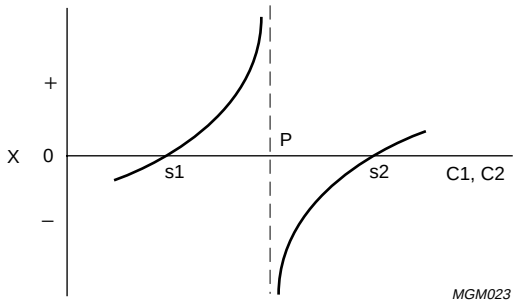
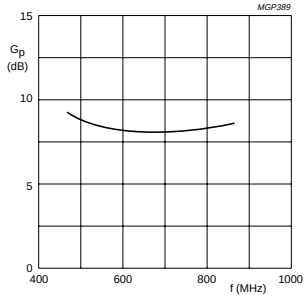


Fig.2-11 Reactance of the reactance unit as a function of C_1 and C_2 ($C_1 = C_2$). s1, s2: first and second series resonances.

2.1.3.4 GAIN AND IMPEDANCE INFORMATION

To facilitate the design of both narrowband and wideband amplifiers, graphs of input impedance, optimum load impedance and power gain over a wide range of frequencies are published in Philips' data sheets, see Fig.2-8 (Figs 10 and 11) and Fig.2-12. The published data are valid for the specified supply voltage and output power; when the conditions in your application are different, please contact Philips Semiconductors for additional information.



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.12 Power gain as a function of load power; typical values.

Fig.2-12 Part of the BLV59 data sheet showing additional information to assist in the design of narrow and wideband amplifiers. See also Fig.2-8.

2.2 MOS devices

2.2.1 Limiting values (Ratings)

As an example, consider the published data (Fig.2-13) for the BLF544, a silicon n-channel enhancement mode vertical DMOS transistor intended for wideband operation in the VHF/UHF range. At 500 MHz and a supply voltage of 28 V, the BLF544 has a specified output power of 20 W.

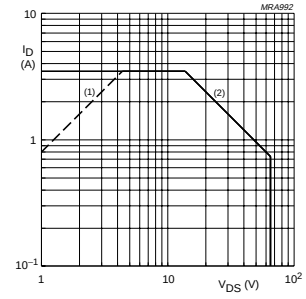
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	48	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

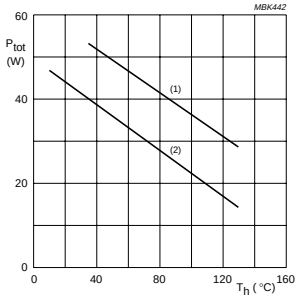
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

Fig.2-13 Part of the BLF544 data sheet showing how the device *ratings* of a MOS transistor are specified.

2.2.1.1 DEFINITIONS

Since many of the ratings of a MOS transmitting transistor are the same or very similar to those of a bipolar device, we shall discuss only the main differences, namely:

V_{DS} *Drain-source voltage*
This is equivalent to V_{CBO} for a bipolar transistor. A quantity like V_{CEO} does not exist for MOS devices.

V_{GS} *Gate-source voltage.*
This rating must be carefully adhered to. Even very small amounts of energy are able to destroy a MOS device. Static charges in particular are dangerous in this respect; ESD protection measures are essential when handling MOS transistors.

I_D *Drain current.*
This is equivalent to I_C for a bipolar transistor.

All other ratings in Fig.2-13 have the same meaning as those for bipolar transistors. Unlike bipolars however, there is no difference between the power dissipation for DC and RF operation. In the DC SOAR, there is an extra drain current limitation at low drain voltages due to $R_{DS\ (on)}$.

2.2.2 Characteristics

As the example of Fig.2-14 shows, the published data contains some well-known parameters such as breakdown voltage and leakage currents and, in addition:

$V_{GS(th)}$ *The gate voltage at which drain current starts to flow.*
As there is quite a large spread on this parameter, matched pairs of some transistor types are available for push-pull operation ($V_{GS(th)}$ matched to within <100 mV).

g_{fs} *The forward transconductance.*
This is the slope of the I_D versus V_{GS} characteristic at a specified I_D. This parameter is important for the power gain of a transistor.

$R_{DS\ (on)}$ *The total resistance in the drain-source circuit at a high, positive V_{GS}.*
$R_{DS\ (on)}$ is the main parameter that determines the drain efficiency.

C_{is} *The input capacitance when the output is short-circuited.*
This means that $C_{is} = C_{gs} + C_{gd}$ where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances respectively.

C_{os} *The output capacitance when the input is short-circuited.*
This means that $C_{os} = C_{ds} + C_{gd}$ where C_{ds} and C_{gd} are the drain-source and gate-drain capacitances respectively.

C_{rs} *The feedback capacitance.*
This is the same as C_{gd}.

I_{DSX} *The maximum drain current that the device can deliver.*
Above I_{DSX}, the transconductance is too low for practical use.

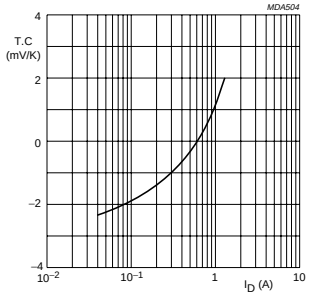
Besides the above, some graphs are given such as I_D versus V_{GS}. As this characteristic is temperature dependent, its temperature coefficient (useful when designing bias units) is given in a separate graph (see Fig.2-14).

$R_{DS(on)}$ is also dependent on junction temperature and this is shown in a graph (see Fig.2-15) Finally, the capacitances are given as functions of the drain voltage (also shown in Fig.2-15). Note, C_{is} is the sum of the gate-source capacitance and the gate-drain capacitance (equal to C_{rs}), and subtracting the latter from C_{is} shows that the gate-source capacitance is almost constant.

CHARACTERISTICS

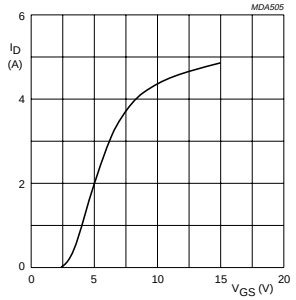
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
ΔV_{GSth}	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
R_{DSon}	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



V_{DS} = 10 V.

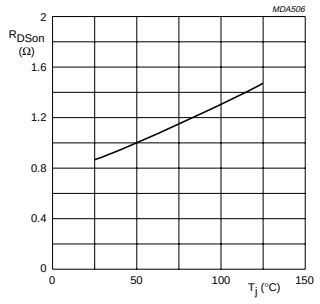
Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



V_{DS} = 10 V; T_j = 25 °C.

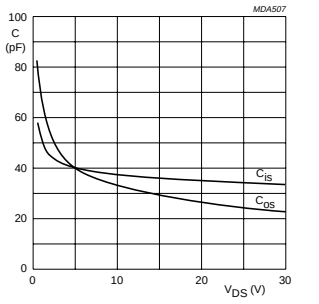
Fig.5 Drain current as a function of gate-source voltage; typical values.

Fig.2-14 Part of the BLF544 data sheet showing how the device *characteristics* of a MOS transistor are specified.



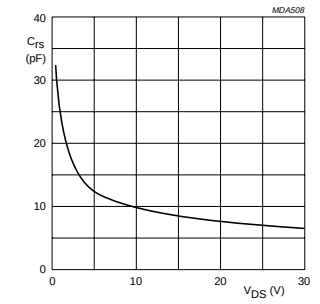
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

Fig.2-15 Part of the BLF544 data sheet showing the $R_{DS(on)}$ and capacitance graphs.

2.2.3 Application information

The published application information for MOS transistors is so similar to that for bipolar devices (see Section 2.1.3), that no further comment is needed here.

2.3 Reliability

Reliability is a measure of the ability of a device to perform its intended function over its useful lifetime under stated conditions. It is thus a measure of the quality remaining after some time and after exposure to certain operating stresses. Like other measures of quality, reliability is a probability. The failure rates of many semiconductors follow the well-known bath-tub curve, (see Fig.2-16).

2.3.1 Failure rate

The instantaneous failure rate is the sum of three components:

Early failures (infant mortalities)
These are failures of devices that initially meet the specification, but which fail due to minor latent defects exposed during the first hours of operation. Such failures are common to the fabrication processes of all semiconductor manufacturers. They can be isolated by subjecting all devices to a burn-in period.

Random failures
This is the dominant failure mode during the main period of life. Failures may occur randomly for no apparent reason. The failure rate is virtually constant during this period, the only one therefore where it is useful to specify a failure rate.

Wear-out failures
These are the increasing number of failures that occur as physical and chemical degradation processes accelerate until no working components remain.

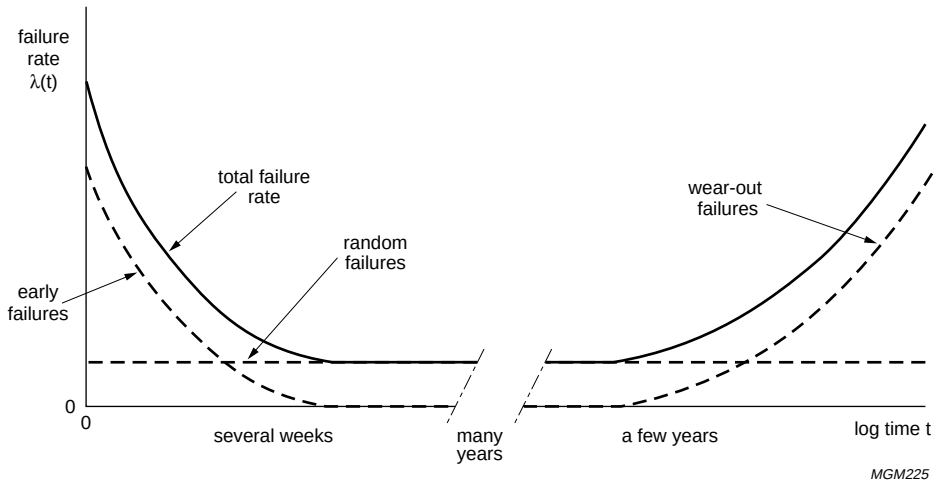


Fig.2-16 The familiar bath-tub curve of failure rate as a function of time. Note, time is given on a log scale - the period of constant failure rate is soon reached.

2.3.2 Mean-Time-To-Failure (MTTF)

During the constant failure rate period, the reliability is:
$R(t) = e^{-\lambda t}$
where:
R(t) is the probability of no failures up to time t, and
λ is the failure rate.

The MTTF is the time after which R(t) has fallen to 37% (1/e), that is, MTTF = $1/\lambda$. A device that has operated up to the MTTF therefore has a probability of survival of 0.37.

2.3.3 Median-Time-To-Failure (MTF or $t_{50\%}$)

In many instances, the cumulative failures of semiconductor devices follow a lognormal distribution. The time at which 50% of the components have failed due to wearout is called the median-time-to-failure. Note that knowledge of MTF is of little value to equipment designers; much more important, and useful, is the likely time to failure of, for example, the first 0.1% ($t_{0.1\%}$).

2.3.4 Bonding wires, metallization and barrier layers

Philips' modern range of RF transmitting transistors with gold bonding wires, gold metallization and a TiPt barrier layer (to prevent gold-silicon alloy formation) are extremely reliable especially at high junction temperatures. The use of barrier layers has enabled the potential reliability of all-gold designs to be fully exploited, and has overcome the shortcomings of all-aluminium designs such as electromigration, aluminium diffusion and thermal fatigue, and the 'purple plague' of the now-obsolete gold-aluminium hybrids.

A two-layer structure formed by depositing a platinum barrier layer on top of a titanium adhesive layer (the latter deposited on the silicon die) has proved to be highly effective at preventing alloy formation. Moreover, as the electromigration of gold is about one tenth that of aluminium, the current density in the metallization is no longer the limiting factor. And, the MTF of 'gold' transistors with barrier layers is theoretically 10^6 to 10^7 hours at a junction temperature of 200 °C. Accelerated life tests have shown that the lifetime mentioned can indeed be reached.

Published MTFs
Note, when comparing the published MTFs of different manufacturers, remember that different manufacturers base their MTFs on different failure mechanisms. Philips, for instance, includes the diffusion of gold into the die silicon, which indicates the quality of the platinum barrier layer, as a failure mechanism. Some manufacturers use electromigration measurements which can *suggest* reliability superior to that obtained using the former, more exacting, criterion.

2.3.5 Power temperature-derating

Finally, it is important to bear in mind the effect of derating. Suppose that an RF amplifier circuit has been designed such that the maximum junction temperature of the output transistor is 200 °C at maximum supply voltage and ambient temperature. This means that for most of the time, under normal operating conditions, the junction temperature will be lower, and the life of the transistor will be longer - more than double (2.4×) per 10 °C reduction in junction temperature.

3 POWER AMPLIFIER DESIGN

3.1 Classes of operation and biasing

3.1.1 Class-A

Class-A operation is characterized by a constant DC collector (or drain) voltage and current. This class of operation is required for linear amplifiers with severe linearity requirements including:

– Drivers in SSB transmitters where a 2-tone 3rd-order intermodulation of at least –40 dB is required

– Drivers in TV transmitters where the contribution to the gain compression must be very low, i.e. not more than a few tenths of a dB

– All stages of TV transposers. These are tested with a 3-tone signal and the 3rd-order intermodulation products must be below –55 to –60 dB. The driver stages should only deliver a small contribution to the overall intermodulation, so they have to operate at even lower efficiency than the final stage (as this is the only way to reduce distortion in class-A).

Though the theoretical maximum efficiency of a class-A amplifier is 50%, because of linearity requirements, the efficiency in the first two applications listed above will be no more than about 25%. And in TV transposers, the efficiency is only about 15% for the final stage and even less for the driver stages.

The transistor power gain in a class-A amplifier is about 3 to 4 dB higher than that of the same transistor operating in class-B. This is because the conduction period of the drain current in class-A is 360° and in class-B only 180° (electrical degrees). Therefore, the effective trans-conductance in class-B is only half that in class-A.

3.1.1.1 DISTORTION

SSB modulation is mainly used in the HF range: 1.5 to 30 MHz. When testing transistors for this application, Philips uses a standard test frequency of 28 MHz. Owing to its variable amplitude, an SSB signal is sensitive to distortion.

3.1.1.1.1 2-TONE INTERMODULATION DISTORTION TEST

3rd and 5th-order products

This is the most common distortion test. In this test, two equal-amplitude tones 1 kHz apart are applied to the input of the amplifier under test. Practical amplifiers will never be completely linear, and the most important distortion products they produce are the 3rd and 5th order ones, because these are in or very near to the pass-band.

NOTE TO SECTION 3

For clarity in equations, identifiers such as R1, +jB2, –jX3 in drawings are written as R_1, $+jB_2$, $-jX_3$ in the body text.

If the frequencies of the two input tones are denoted by p and q, the 3rd-order products are at frequencies of 2p–q and 2q–p, see Fig.3-1. The 5th-order products which usually have smaller amplitudes are at 3p–2q and 3q–2p. Note, the two intermodulation products of the same order don't necessarily have equal amplitudes. This can be due to non-ideal decoupling of the supply voltages, i.e. decoupling that is insufficiently effective at all the frequencies involved. Philips publishes the largest value in data sheets.

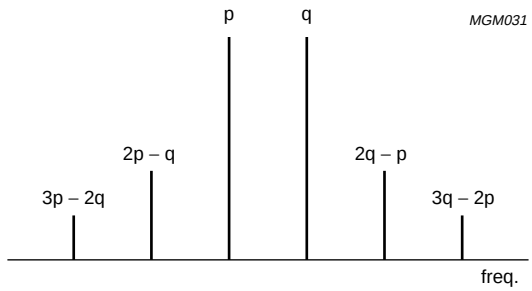


Fig.3-1 Position of the main intermodulation distortion products in the 2-tone test where p and q are the input tones.

Power relationships

If the tones at p and q are each of 10 W, then the combination has an *average (calorific)* power of 20 W. The two tones can however combine in phase or out of phase, producing an RF signal of variable amplitude. When the two tones are in phase, the voltage amplitude is twice that of one tone, so the power is four times that of one tone (in this example: 40 W). This maximum power is called the peak envelope power (PEP) and is commonly published in data sheets. When the two tones are in anti-phase, their combined amplitude is zero. In the ideal case, i.e. with no distortion, the envelope of the combined signal consists of half sine waves, see Fig.3-2.

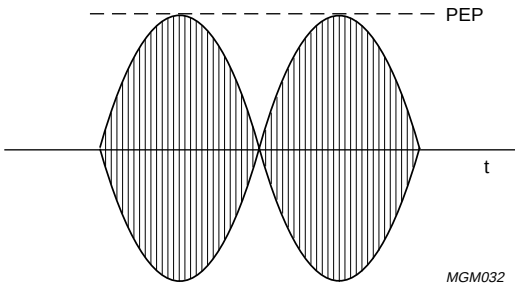


Fig.3-2 Two-tone signal showing the peak envelope power.

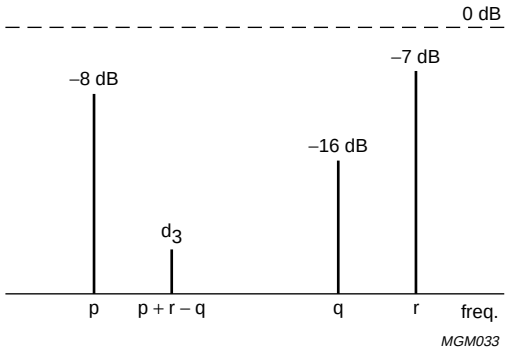


Fig.3-3 Three-tone test. The 3rd-order intermodulation product, d_3, is at p+r–q.

In class-A applications, distortion products are nearly always specified relative to the amplitude of one of the input test tones. As a general guideline, in the linear region of a class-A amplifier, every 1 dB reduction of output power reduces 3rd-order intermodulation distortion by 2 dB.

3.1.1.1.2 3-TONE TEST FOR TV TRANSPOSER APPLICATIONS

In a TV transposer, vision and sound are amplified together, so the distortion requirements are more severe, and it is usual to measure intermodulation using a 3-tone signal. The most popular test (DIN 45004B, para.6.3: 3-tone uses tones of –8 dB, –16 dB and –7 dB with respect to a 0 dB reference power level called the peak sync power. The first tone (–8 dB) represents the vision carrier, the second (–16 dB) a sideband, e.g. the colour carrier, and the third (–7 dB) the sound carrier. This combination of tones has a real peak power which is very close to the 0 dB level, namely: +0.02844 dB or +0.66%.

Another important relationship is the ratio of the average power to the 0 dB level. This ratio is 0.3831, so the 0 dB level is found by multiplying the calorific power by 2.61.

In the 3-tone test, the frequency of the –7 dB tone is 5.5 MHz higher than that of the –8 dB tone, while the frequency of the –16 dB tone is varied between the other two to produce the most intermodulation. If the frequencies of the tones are denoted by p, q and r respectively, we are primarily interested in the 3rd-order intermodulation product p+r–q which is inside the passband and which, in addition, usually has the largest amplitude, see Fig.3-3.

The test requirement for this product for a *complete* transposer is –51 dB with respect to the 0 dB reference level. This implies that the requirements for final stages are more severe (typically –55 dB) while those for driver stages more severe still (typically –60 dB).

In another 3-tone test method, the amplitude of the audio carrier is reduced from –7 dB to –10 dB. This has several effects:

– The actual peak power is only 76.2% of the 0 dB level
– The calorific power is 28.36% of the 0 dB level
– The intermodulation requirements are more severe. Because one of the tones is reduced by 3 dB, the intermodulation product at f_{p+r-q} is also reduced by 3 dB provided the amplifier is operating in the linear region.

3.1.1.1.3 RELATIONSHIP BETWEEN 2- AND 3-TONE TEST RESULTS

Theoretically, the first-mentioned 3-tone test and the 2-tone test measurement of SSB amplifiers are related. When (but only when) the PEP of the 2-tone test and the 0 dB level of the 3-tone test are equal, there is always a 13 dB difference in the intermodulation distortion. For example, if, an intermodulation of –40 dB is measured in the 2-tone test, –53 dB will be measured in the 3-tone test. Further, the 2-tone intermodulation should be measured relative to the two equal-amplitude tones and the 3-tone intermodulation relative to the 0 dB level.

Class-A amplifiers for TV transposers and transmitters behave in a similar way to those for SSB driver stages. So, reducing the output power by 1 dB reduces 3rd-order intermodulation by 2 dB.

3.1.1.2 BIASING

For MOS transistors, biasing is very simple. The temperature coefficient of the I_D versus V_{GS} curve is almost zero at the optimum operating point so an adjustable resistive divider is sufficient. For bipolar transistors, the situation is more complicated because of the temperature dependency of h_{FE} and V_{BE}.

In an audio amplifier, it is usual to stabilize the operating point by means of an emitter resistor and a base potentiometer. In an RF amplifier, however, it is preferable to ground the emitter to obtain maximum power gain as illustrated in Fig.3-4.

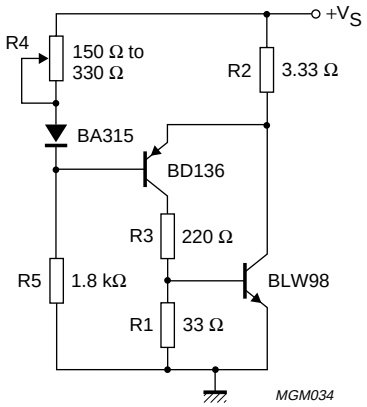


Fig.3-4 Class-A biasing circuit with grounded emitter for maximum power gain.

3.1.1.2.1 DESIGN EXAMPLE

In this example, a bias circuit must be designed such that the BLW98 RF transistor operates at V_{CE} = 25 V and I_C = 850 mA. The auxiliary transistor is a small PNP audio power transistor: BD136. Owing to the large negative feedback in the final circuit (Fig.3-4), the operating point of the BLW98 is extremely well stabilized for variations in ambient temperature and for the h_{FE} spread of the BLW98.

For instance, if h_{FE} rises due to an increase in ambient temperature, the collector voltage of the BLW98 will fall slightly, causing a decrease in the collector current of the BD136 and therefore in the base current of the BLW98.

The BA315 diode is used to compensate the temperature coefficient of the V_{BE} of the BD136. The variable resistor in series with this diode serves to adjust the I_C of the BLW98 accurately at the desired value.

3.1.1.2.2 CALCULATION OF COMPONENT VALUES

BD136 collector current

The supply voltage is chosen 2 to 3 V higher than the V_{CE} of the BLW98, e.g. 28 V (to provide sufficient negative feedback). The h_{FE} of the BLW98 can vary from 15 to about 100. To reduce the I_C variation of the BD136, the BLW98 is pre-loaded with a resistor between base and emitter (R_1 in Fig.3-4). The I_B of the BLW98 can vary from 8.5 to 57 mA while the required V_{BE} for an I_C of 850 mA is about 0.98 V. If 30 mA flows through R_1, the required resistance is: 0.98/0.03 ~ 33 Ω.

The I_C of the BD136 can now range from 38.5 to 87 mA with an average value of 51 mA. The BD136 has a typical h_{FE} of 100, so its I_B is approximately 0.5 mA and its average emitter current is 51.5 mA. The current through the collector resistor, R_2, of the BLW98 is then: 0.85 + 0.0515 = 0.9015 A. For a voltage drop of 3 V (28 – 25 V), a 3.33 Ω resistor (3/0.9015) rated at a rather high 2.7 W (3×0.9015) is required.

Protection resistor

To protect the BLW98 and to reduce the dissipation in the BD136, a resistor, R_3, is included between the collector of the BD136 and the base of the BLW98. The value of R_3 must be calculated on the basis of the minimum h_{FE} of the BLW98, and thus on the maximum I_C of the BD136 of 87 mA. As the V_{BE} of the BLW98 is about 1 V and the $V_{CE(sat)}$ of the BD136 is less than 1 V, the maximum voltage drop across R_3 must be less than 23 V. This means a maximum value of: 23/0.087 = 264 Ω, say 220 Ω, and the maximum dissipation in R_3 is $0.087^2 \times 220 = 1.67$ W.

Base potentiometer

Finally, the BD136 base potentiometer components (R_4, R_5 and the BA315) have to be determined. The potentiometer current must be high compared with the I_B of the BD136 (say 10 to 20 I_B); 13 mA is suitable and corresponds with the test circuit in the data sheet. As the V_{BE} of the BD136 is about 0.7 V and the voltage drop across the BA315 diode is 0.8 V, there is a drop of 2.9 V across the variable resistor, so a nominal resistance of 2.9/0.013 = 223 Ω is required. A range of 150 to 330 Ω provides sufficient adjustment for practical use. Across resistor R_5, there is a voltage drop of 24.3 V and a current of 13.5 mA, so a resistance of 24.3/0.0135 = 1.8 kΩ is required.

Note, unlike some types of bias circuit, this type does not suffer from parasitic oscillations due to high loop gain.

3.1.2 Class-AB

Class-AB operation is characterized by a constant collector voltage and (unlike class-A) a quiescent collector current that increases with drive power. The distortion behaviour is also different to that of class-A. Class-AB operation is used for linear amplifiers with less severe requirements including:

– Final stages of SSB transmitters where a 2-tone *3rd*-order intermodulation of about –30 dB is required
– Final stages of TV transmitters where a gain compression of max. 1 dB is required
– Final stages of base stations for cellular radio.

Maximum efficiency is obtained at maximum power, and although the theoretical maximum efficiency of a class-AB amplifier is 78.5%, in practice it is always lower because:

– There are resistive losses both in the transistor and in the output matching circuit
– The collector AC voltage cannot be driven to its maximum value because of distortion requirements
– There is a small quiescent current (for a bipolar transistor, about 2% of the collector current at maximum power and, for a MOSFET, about 12% of the drain current at maximum power).

For HF and VHF amplifiers, in a 2-tone situation, the average efficiency is about 40% which corresponds to an efficiency of 60 to 65% at maximum power (PEP situation). At higher frequencies, the efficiencies are somewhat lower. The power gain of a class-AB amplifier is between those of class-A and class-B amplifiers.

3.1.2.1 DISTORTION

Unlike a class-A amplifier where intermodulation improves as the power is reduced, for a class-AB amplifier, the distortion is as shown in Fig.3-5.

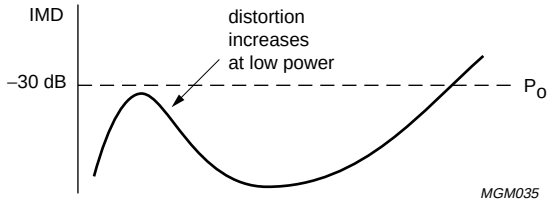


Fig.3-5 Intermodulation distortion as a function of output power for a class-AB amplifier.

The increasing distortion at low powers is due to ‘cross-over’ distortion, i.e., distortion during the transition from class-A to class-B operation.

3.1.2.1.1 EFFECT OF LOAD IMPEDANCE

An important factor affecting distortion is the load impedance. The optimum value at the fundamental frequency is always specified in Philips’ transistor data sheets for the frequency range of interest. The load reactance at the second harmonic is also important. Often, this is solely the output capacitance of the transistor. The collector or drain current contains a substantial second harmonic component which due to the presence of the load reactance causes a second harmonic output voltage component. A relatively small component can be tolerated. However, if it is above say 10% of the voltage at the fundamental frequency, the amplifier will saturate at a lower power than intended, so the allowable distortion is reached at lower power.

This can be solved by adding an external capacitor between collector (or drain) and earth. Though this will reduce gain and efficiency somewhat, it will reduce intermodulation significantly. A good practical rule is that the reactance of the parallel combination of internal and external capacitance at the second harmonic should be about 2.2 times the load resistance at the fundamental frequency. For wideband amplifiers, there is another solution which can be found in application reports, e.g. *“NCO8703”*.

3.1.2.2 BIASING

For MOS transistors, biasing is rather easy. In most cases, a resistive voltage divider is sufficient. If necessary, a diode or an NTC thermistor can be included in the lower branch to compensate for the negative t.c. of the gate voltage.

For bipolar transistors, a more sophisticated circuit is required. The circuit has to deliver a constant voltage of about 0.7 V (adjustable over a restricted range) and should have very low internal resistance. The latter is required to accommodate a wide range of ‘load’ currents (i.e. base drive currents for the RF transistor), whilst maintaining a nearly constant output voltage. Other desired properties are temperature compensation and the lowest possible current consumption. Figure 3-6 shows a circuit meeting these requirements.

The bias circuit has large negative feedback. If the load current increases, the output voltage drops slightly, decreasing the collector current of the BD135 whose collector voltage increases to counteract the drop in output voltage.

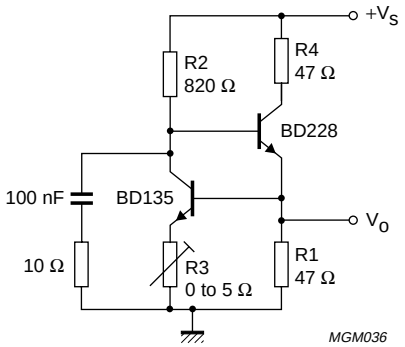


Fig.3-6 Bias circuit for a class-AB bipolar transistor amplifier.

3.1.2.2.1 DESIGN EXAMPLE

Calculation of component values

BD228 BASE AND COLLECTOR CURRENT

In this example, it is assumed that the bias circuit is for an amplifier delivering an output power of 100 W at a supply voltage of 28 V. So, if the minimum amplifier efficiency is 50%, the required DC input power is 200 W, corresponding to a collector current of 7.14 A. If the transistors used have a minimum h_{FE} of 15, the maximum base current can be 0.48 A. Such an amplifier could be the final stage of an SSB transmitter where the output power and therefore also the base current vary from almost zero to 0.48 A. In the bias circuit, a pre-loading resistor, R_1, is used to reduce the base current variations. To draw 15 mA at 0.7 V, R_1 must be 0.7/0.015 = 47 Ω. The maximum emitter current of the BD228 will then be nearly 0.5 A. From the published h_{FE} data for this type, the base current is 15 mA maximum.

The current through the collector resistor, R_2, of the BD135 is chosen to be twice this value, i.e. 30 mA, to restrict the variations in the collector current of the BD135. The V_{BE} of the BD228 is about 0.8 V, so the voltage across R_2 is 26.5 V, giving a value of: 26.5/0.03 = 883 Ω (nearest preferred value: 820 Ω, 1 W.)

OUTPUT VOLTAGE

At first sight, the choice of a BD135 in this circuit seems a bit overspecified for a transistor that has to draw only 30 mA. Yet this has been done deliberately because then the V_{BE} required by the BD135 is low (smaller than the bias voltage to be delivered to the RF amplifier.) The difference is corrected by the variable resistor, R_3, in the emitter of the BD135. The output voltage of the bias circuit, and thus the quiescent current of the RF amplifier, can now be adjusted. With a resistor of 5 Ω max., the output voltage can be adjusted by at least 100 mV, sufficient for this application.

PROTECTION RESISTOR

To protect the BD228 against the consequences of a short-circuit of the output voltage, it is advisable to include a resistor, R_4, in the collector lead. As the BD228 has a $V_{CE(sat)}$ of 0.8 V max., a voltage drop of 26.5 V across R_4 is allowed at the maximum collector current of 0.5 A. The maximum value of this resistor is therefore 26.5/0.5 = 53 Ω (nearest preferred value: 47 Ω.) Note that R_4 must be rated at 12 W ($I^2R = 0.5^2 \times 47 = 11.75$).

PERFORMANCE

The internal resistance of this bias circuit is exceptionally small. Values of less than 0.1 Ω have been measured, so the output voltage varies by less than 50 mV from zero to full load. The value of the output voltage is mainly determined by the V_{BE} of the BD135, which has a well-known temperature dependence (about −2 mV/°C), providing reasonable matching with the required V_{BE} of RF transistors without any special measures.

This type of bias circuit can develop parasitic oscillations near 1 MHz with highly capacitive loads (such as the supply decoupling capacitors in the RF circuit). This can be prevented by an RC combination between the collector of the BD135 and ground. Good values are 10 Ω and 100 nF.

3.1.3 Class-B

This class of operation can be used for all RF power amplifiers without linearity requirements, e.g. in portable and mobile radios, base stations (except those for the 900 MHz band) and FM broadcast transmitters.

For bipolar transistors, no biasing is required, i.e. V_{BE} = 0, while MOSFETS are used with very small quiescent drain current, say 2 to 3% of the current at full power. This can be provided in the same way as for class-AB amplifiers.

The collector (or drain) efficiency is about 70% at VHF, while the power gain depends on the frequency of operation.

3.1.4 Class-C

This class of operation is *not recommended for bipolar transistors,* because it shortens transistor life, see also Section 2.1.1: V_{EBO} rating. An exception can be made for

a very small negative bias (<100 mV) which can be generated with a small resistor between base and emitter.

MOSFETS are more tolerant in this respect and can be adjusted at V_{GS} = 0, causing only a few dB reduction of power gain. This is not a problem in most cases because the gain is rather high. The main advantage is a higher drain efficiency. A good example is the BLF278 which at 108 MHz in class-B gives 70% efficiency at 22 dB gain, and in class-C, 80% efficiency at 18 dB gain.

3.1.5 Class-E

This class of operation is discussed in more detail in application report *"COE82101"*. With an optimum choice of component values for the output matching network of the transistor, collector or drain efficiencies of 85% can be reached. However, the use of class-E is restricted as beyond 60 to 70 MHz, efficiency falls significantly.

3.1.6 Influence of driver stages on intermodulation

Most linear amplifiers (i.e. class-A and class-AB) consist of a cascade of two or more amplifier stages. The overall distortion is mainly caused by the final stage because the driver stages are generally designed to have a lower distortion. In fact, attention to the design of the driver stage will pay dividends in overall performance as the following analysis illustrates.

The total distortion of a multi-stage amplifier, d_{tot}, can be determined from:

$$d_{tot} = 20 \log\left(10^{d_1/20} + 10^{d_2/20} + ... \right)$$

where d_1, d_2 etc. are the intermodulation products of each stage in dB.

With two stages, e.g. driver plus a final stage, it is useful to know by how many dB the overall distortion worsens for a given difference in distortion between driver and final stage (assuming the driver distortion is the smaller). This relationship is described by:

$$B = 20 \log\left(1 + 10^{-A/20} \right)$$

where:
A is the absolute difference in distortion between driver and final stage, and
B is the increase in distortion in the output of the amplifier.

This relationship is summarized in Table 3-1 for a few values. Clearly, if a large increase in distortion is unacceptable, the driver stage has to be substantially better than the final stage.

Table 3-1 Effect of driver distortion upon overall distortion

A	**B**
Amount by which driver IMD is superior to final stage IMD (dB)	Increase in IMD of output amp. (dB)
0	6.0
5	3.9
10	2.4
15	1.4
20	0.8

3.2 Matching

3.2.1 Narrow-band (test) circuits

NARROW-BAND MATCHING CIRCUITS

- *Section 3.2.1.1:* describes the principles of impedance matching
- *Section 3.2.1.2:* describes two types of adjustable network, and how to handle high power levels
- *Section 3.2.1.3:* deals with UHF versions of the networks of the previous section using striplines
- *Section 3.2.1.4:* discusses the double networks required for very-low transistor impedances
- *Section 3.2.1.5:* is on π-networks where the trimmers are grounded on one side to avoid 'hand effects'. VHF and UHF versions are given as well as the modifications for low-impedance transistors.

3.2.1.1 GENERAL REQUIREMENTS

Every transistor amplifier needs to be impedance matched both at its input and output. In test circuits, the 50 Ω signal source must be matched to the complex input impedance of the transistor. At the output, the reverse is needed, namely, the 50 Ω load resistance must be transformed to the optimum complex load impedance of the transistor.

In multistage amplifiers, networks are required in addition, to provide direct matching between two complex impedances. The most important requirement for all matching networks is that power losses must be minimized. In addition, especially for output networks, the

voltage and current loading of the components must be taken into account.

Most matching networks have to be tunable, ideally with a large tuning range and with smooth, continuous control. Unfortunately, these are conflicting requirements so a compromise must be made.

In general, there are no severe requirements on the bandwidth of a matching network. However, it can be advantageous not to make this bandwidth too small, thereby improving the smoothness of the alignment and reducing losses.

The objective of matching is to maximize power transfer. This requires that the source and load impedances are complex conjugates, i.e. they have equal resistance components, and equal reactance components but of opposite sign.

The simplest form of matching between a source with a real (i.e. resistive) internal impedance and a different load resistance can be made using two reactive elements, see Fig.3-7.

In Fig.3-7, A and B have low-pass characteristics and are most commonly used because of their suppression of harmonic components. C and D have high-pass characteristics and, although used less frequently, have advantages in specific cases such as interstage networks.

The higher resistance is denoted by R_h and the lower by R_l. R_h always has a parallel reactance (X_p) and R_l a series one with opposite sign (X_s).

The component values can be easily calculated from:

$$\frac{X_S}{R_l} = Q = \frac{R_h}{X_p} \quad \textbf{(1)}$$

and

$$\frac{R_h}{R_l} = Q^2 + 1 \quad \textbf{(2)}$$

where Q is the *loaded* Q-factor which has to be small compared with the *unloaded* Q-factor of the components.

Note: Equations (1) and (2) are used on many occasions in subsequent sections to determine component values in networks.

Up to now, we have only considered matching two different value *resistances*. In practice, at least one of the impedances is complex, and in such cases, one of the reactances, namely the one closest to the complex impedance, has to be modified.

Suppose that in Fig.3-7, circuit A is used for the input matching of a transistor. If the transistor's input impedance is capacitive, X_s has to be increased by the absolute value of the transistor's input reactance as Fig.3-8 shows. If the input impedance is inductive, the reverse is needed: X_s has to be reduced by this amount. Note, if in the latter case the input reactance of the transistor is higher than the calculated X_s, the new X_s becomes negative, meaning a capacitor has to be used instead of an inductor.

Similar considerations hold for the other configurations.

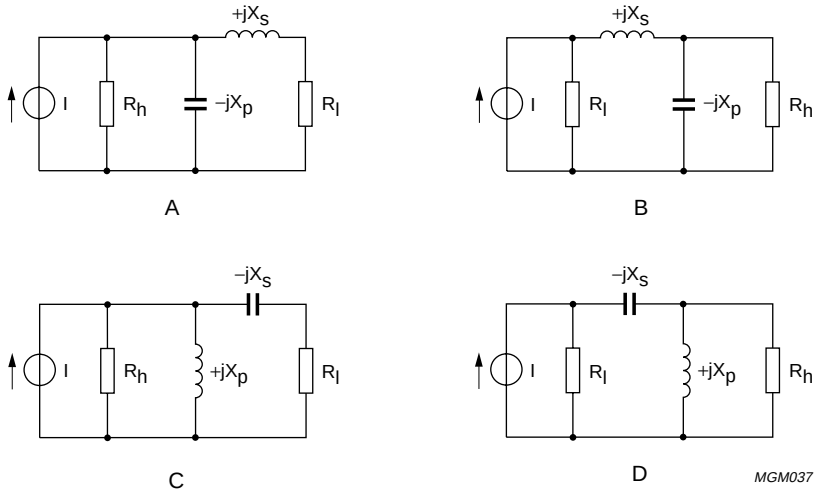


Fig.3-7 Four examples of matching a resistive source and load using two reactive elements.

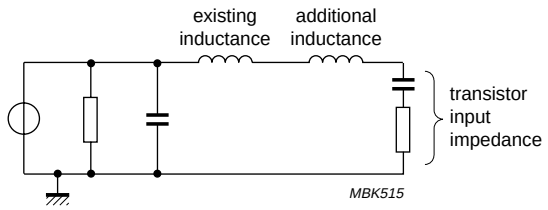


Fig.3-8 Adding a series inductance to the input matching circuit A of Fig.3-7 to compensate for the capacitive part of a transistor's input impedance.

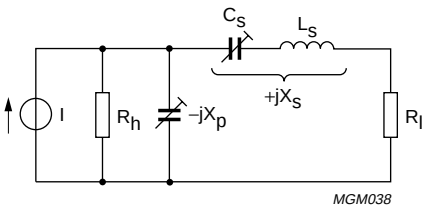


Fig.3-9 Adjustable matching network (based on circuit A of Fig.3-7) suitable for test circuits. A similar network can be made based on circuit B of Fig.3-7.

3.2.1.2 ADJUSTABLE L AND T NETWORKS[1]

Owing to their limited control options, the networks described in the previous section are not really suitable for use in test circuits. This limitation can be overcome in two ways by simple circuit modifications.

3.2.1.2.1 NETWORK 1

Starting from circuits A (high-to-low transformation) and B (low-to-high transformation) of Fig.3-7, X_p is made (partly) variable by using a trimmer (optionally with a fixed capacitor in parallel to lower the trimmer current and for smoother control). In addition, a variable capacitor is connected in series with X_s such that the combination remains inductive. (C_s can again be the parallel combination of a trimmer and a fixed capacitor). This means the inductance has to be increased to keep the combination's reactance at the calculated value of X_s, see Fig.3-9.

For the modified network, the new Q-factor for L_s is

$$Q' = \frac{\omega L_s}{R_l}$$

And since L_s has increased, Q' is higher than the Q defined in the previous section, meaning the circuit losses are higher and the bandwidth is lower. Therefore, these effects must be reduced as much as possible by restricting the increase in L_s.

3.2.1.2.2 NETWORK 2

A variant of network 1 is shown in Fig.3-10. This circuit uses smaller capacitances than the circuit of Fig.3-9. And though the harmonic suppression is worse, this can usually be tolerated in input networks.

The calculation of component values is done in two stages. To assist understanding, it is best to imagine this circuit as two cascaded sections (D plus A from Fig.3-7), see Fig.3-11. The first section transforms R_h to a higher value at point A, and the second transforms this value down to R_l. To restrict the losses and reduction of bandwidth, it is advisable to choose the equivalent parallel resistance at point A no higher than necessary. When making the calculation, note that the combined reactance of L_p' and C_p' is always negative (C_p' dominates), so the combination can be realized by a (variable) capacitor.

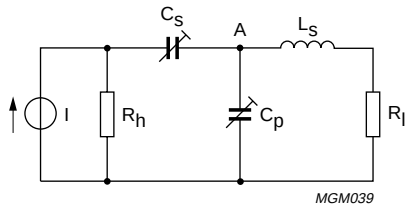


Fig.3-10 Variant of the matching network shown in Fig.3-9.

(1) Note: Many of the networks in Section 3.2 are 'reversible'.

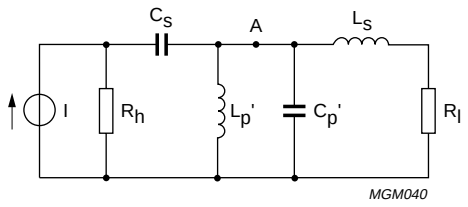


Fig.3-11 The matching network of Fig.3-10 represented as two cascaded sections to simplify calculation.

Another possibility is a combination of networks 1 and 2. This is sometimes used in output networks that must handle relatively high power, see Fig.3-12.

The purpose of C_{p1} is to drain some, say half, of the RF current to ground so that the current through C_s and C_{p2} becomes proportionally smaller, allowing components of a lower rating to be used.

The equivalent parallel resistance at point A should be 2 to 3 times R_h which determines the value of L_s (from equations (1) and (2), the resistance ratio determines the Q, and $X_s = QR_l$). Next, choose a value for C_{p1} that is about half that required to transform R_l to the resistance at point A.

Looking from point A to the left (but including C_{p1}), we see an inductive impedance: R + jX, where $R > R_l$. The remaining part of the calculation is then the same as for network 1.

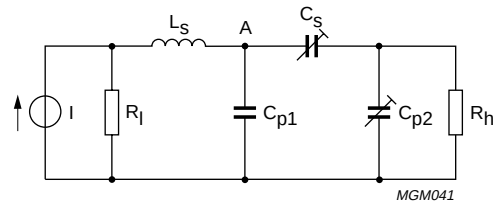


Fig.3-12 Matching network formed by combining those shown in Figs.3-9 and 3-10.

With these and the following networks, it is often needed to transform an impedance from series to parallel components or vice versa. For such transformations, the equations given in the previous section for calculating L-networks can be used with R_l as the series resistance component and R_h as the parallel resistance component.

3.2.1.3 UHF NETWORKS

Above 300 MHz, it is not very practical to work with coils, so transmission lines in the form of striplines are preferred, see Fig.3-13. As well as having series inductance, striplines have parallel capacitance which transforms the real part of the load impedance, calling for a modified calculation.

Figure 3-13 is very similar to the right-hand part of the circuit shown in Fig.3-10. The (low) load impedance is known, but note that its imaginary part can be positive or negative depending on the transistor. And R_{ip} is chosen in the same manner as the resistance at point A in network 2, Section 3.2.1.2.

Next, choose the characteristic resistance of the stripline to satisfy the condition:

$$R_c > \sqrt{R_{ls} R_{ip}}$$

The exact value of R_c is set by practical considerations as both very narrow and very broad striplines are undesirable.

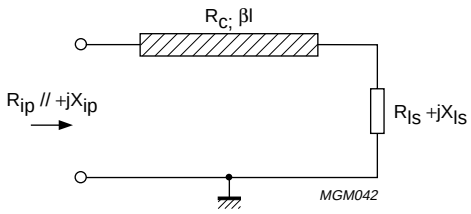


Fig.3-13 Representation of a stripline used in UHF matching networks.

It's now possible to calculate the electrical length (βl) and the parallel input reactance (X_{ip}) from the following two equations:

$$\tan \beta l = \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$

where:

$a = R_c^2 - R_{ls}R_{ip}$

$b = 2R_c X_{ls}$

$c = R_{ls}^2 + X_{ls}^2 - R_{ls}R_{ip}$

and:

$$X_{ip} = \frac{R_{ls}R_{ip}}{X_{ls} + \tan \beta l \left(R_c - \frac{R_{ls}R_{ip}}{R_c} \right)}$$

The values of the (variable) capacitors are calculated as described in Section 3.2.1.2.

3.2.1.4 DOUBLE NETWORKS

In some cases, the input and/or load impedance of the transistor is so low that a direct transformation, as just described in Section 3.2.1.3, leads to very high values of the loaded Q-factor with all its negative consequences. It is then better to add an extra (fixed) section as shown in Figs 3-14 and 3-15.

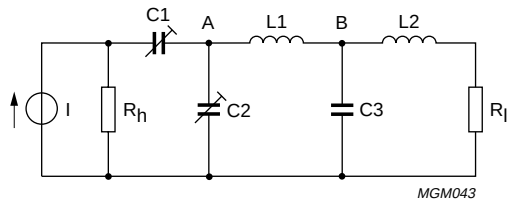


Fig.3-14 Adding a fixed section to the network of Fig.3-10 avoids high loaded Q-factors.

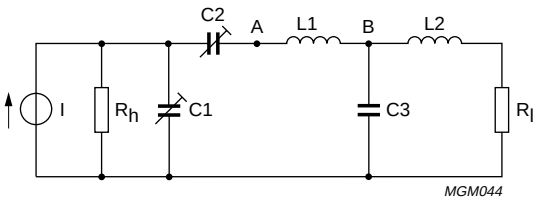


Fig.3-15 Circuit with the fixed section added to the alternative network of Fig.3-9.

Suppose that R_h = 50 Ω and R_l = 1 Ω. A suitable value for the equivalent parallel resistance at point A is then 100 to 150 Ω (i.e. more than 50 Ω, but not so big in view of circuit losses and bandwidth). At point B, a value which is the geometric mean of that at point A (say 125 Ω) and R_l is required, namely $\sqrt{(125 \times 1)}$ = 11.2 Ω.

Without the double network, the loaded Q is:
$\sqrt{(125 - 1)}$ = 11.1

and with the double network, it is :
$\sqrt{(11.2 - 1)}$ = 3.2 which is a significant improvement.

This double network variant also has advantages for output networks. Furthermore, by replacing some or all of the coils by striplines, it can be used at higher frequencies.

3.2.1.5 PI-NETWORKS

3.2.1.5.1 FOR THE VHF RANGE

The networks considered up to now have used both parallel and series capacitors. This can be undesirable because of the so-called 'hand-effect' (the influence of an operator's capacitance) when adjusting a variable capacitor with an RF signal on both sides of it. This effect is present even when an insulated adjuster is used. An alternative method of impedance matching which uses only parallel capacitors overcomes this problem, see Fig.3-16.

If R_l is the low transistor output impedance and R_h the 50 Ω load resistance, then we start by transforming R_l up to about 50 Ω by the fixed section L_1-C_1. This fixed section is followed by a Pi-network C_2-L_2-C_3 which can transform the impedance either up or down as required, and the Pi-network component values are calculated as follows (see Fig.3-17).

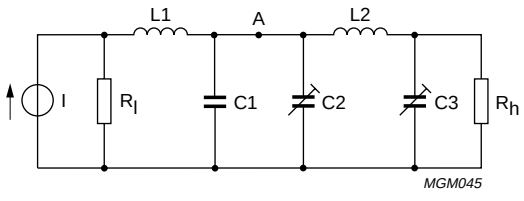


Fig.3-16 Impedance matching circuit using only *parallel* capacitors.
This arrangement in which only one side of the capacitor is 'hot' allows manual tuning on the grounded side of the capacitor, avoiding the 'hand-effect'.

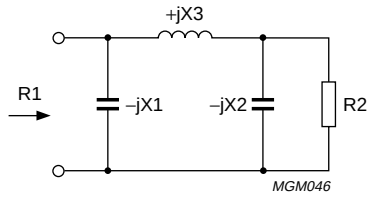


Fig.3-17 Pi-network circuit for the calculation when both R_1 and R_2 have fixed values.

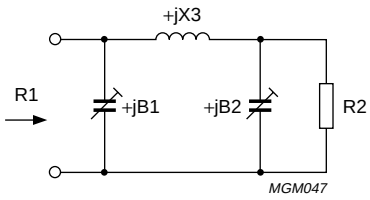


Fig.3-18 Pi-network circuit for the calculation with adjustable input resistance, R_1. R_2 is fixed, e.g. 50 Ω.

For the condition: $X_3 \leq \sqrt{R_1 R_2}$,

$$X_1 = \frac{R_1 X_3}{R_1 + \sqrt{R_1 R_2 - X_3^2}}$$

and

$$X_2 = \frac{R_2 X_3}{R_2 + \sqrt{R_1 R_2 - X_3^2}}$$

In most cases however, we want to adjust the input resistance by varying X_1 and X_2, for example, to suit different transistors and for maximum power transfer. Figure 3-18 shows a suitable network in which, for mathematical convenience, susceptances ($B = \omega C$) have been used instead of reactances.

The value required for X_3 is determined by the minimum value of R_1:

$$X_3 = \sqrt{R_{1\,min} R_2}$$

$$B_{1\,min} = B_{2\,min} = \frac{1}{X_3}$$

$$\Delta B_1 = \frac{1}{2R_{1\,min}}$$

and

$$\Delta B_2 = \frac{\sqrt{\frac{R_{1\,max}}{R_{1\,min}} - 1}}{R_2}$$

So both capacitors have the same minimum value but generally a different control range (Δ).

The losses in this type of Pi-network are in general somewhat higher than those in the networks discussed earlier. The losses increase as the difference between R_1 (avg.) and R_2 increases and as the control range increases since in both cases the loaded Q of the components increases.

The losses can be kept within reasonable limits if the average value of R_1 is within a factor of 2 (up or down) of R_2 (i.e. $R_2/2 < R_1 < 2R_2$). For the control range of R_1, a factor of 4 (total) is generally suitable, providing a control factor of 2 (up and down) from the nominal value.

3.2.1.5.2 FOR THE UHF RANGE

The network just described can also be made in a stripline version, see Fig.3-19.

The characteristic resistance of the stripline must satisfy the condition:

$$R_C > \sqrt{R_{1\,min} R_2}$$

Then the other quantities become:

$$\tan \beta l = \frac{1}{\sqrt{\frac{R_c^2}{R_{1\,min} R_2} - 1}}$$

$$B_{1\,min} = B_{2\,min} = \frac{1}{R_c \tan \beta l}$$

$$\Delta B_1 = \frac{1}{2R_{1\,min}}$$

$$\Delta B_2 = \frac{\sqrt{\frac{R_{1\,max}}{R_{1\,min}} - 1}}{R_2}$$

So clearly this stripline network has much in common with the previous one.

3.2.1.5.3 PI-NETWORK MODIFICATIONS FOR LOW-IMPEDANCE TRANSISTORS

If the transistor impedance is very low (say <5 Ω) as occurs in high power situations, there are two options:

1. Make the average value of R_1 lower than R_2, e.g. half of R_2
2. Use two pre-matching sections instead of one. If this is done, make the impedance between the two sections equal to the geometric mean of the transistor impedance and the average input resistance of the Pi-network.

3.2.2 Wideband circuits

WIDEBAND HF MATCHING CIRCUITS OVERVIEW

HF range *(Section 3.2.2.1)*

– Describes the procedures for input/output matching of MOS and bipolar transistors. Most attention is paid to MOS devices as they are usually the preferred choice for HF applications.

– *Section 3.2.2.1.1* describes some output compensation circuits. Output compensation aims to maintain the ideal load impedance over the frequency band of interest to obtain the highest efficiency and lowest distortion. This section explains:

  * How to compensate a transistor's output capacitance with one or two elements - the latter giving superior results

  * How to compensate parallel inductances such as RF chokes and/or transformer inductance to improve performance at the lower end of the band, and the selection of compensation (coupling) capacitor(s).

– *Section 3.2.2.1.2* deals with the design of input networks to obtain low input VSWR, and high, flat power gain over the whole frequency band.

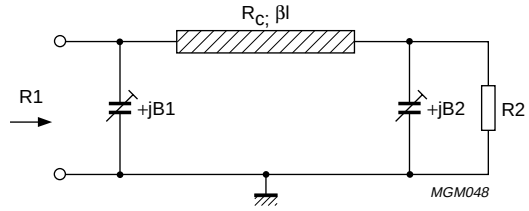


Fig.3-19 Stripline version of the Pi-network of Fig.3-18.

3.2.2.1 THE HF RANGE

This frequency range covers 1.6 to 28 MHz. Most transmitters in this range work with single sideband modulation and wideband power amplifiers. The impedance transformation in these amplifiers can be done either by transmission line type transformers or by compensated conventional transformers (extensively described in application reports *"ECO6907"* and *"ECO7213"*).

In addition, a number of compensation techniques can be used at both output and input. For the former, this is done to obtain maximum output power and efficiency over the whole frequency band; for the latter, it's done to obtain maximum and flat power gain and good impedance matching over the band.

3.2.2.1.1 COMPENSATION AT THE OUTPUT

Compensation of output capacitance

Take as an example the BLF177 MOS transistor. From the published data sheet, this has an output capacitance of 190 pF which rises at full power by about 15% to 220 pF. The capacitor reactance at 28 MHz is about four times the load resistance of 6.25 Ω. Without compensation, the output VSWR is 1.28 which is rather high. To reduce this VSWR, one or two external components can be used. Compensation with one element is shown in Fig.3-20. Two elements will of course give a better result than one, and is described later.

These compensation examples make use of Chebyshev filter theory where it is usual to express the values of the filter elements normalized to a characteristic resistance (source and/or load resistance) of 1 Ω and to a cut-off (angular) frequency, ω, of 1 rad/s. For a low-pass filter, 1 rad/s is the maximum angular frequency, and for a high-pass filter the minimum. Normalized quantities are denoted by g_k where k is a filter-element identifier (Ref.1).

Single-element compensation

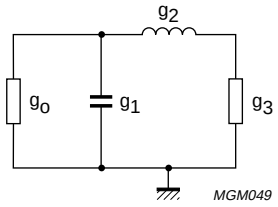


Fig.3-20 Output capacitance compensation using one element.
g_o: optimum load resistance;
g_1: output capacitance of device.

In the circuit of Fig.3-20, the filter elements are:

g_0: the optimum load resistance (known);

g_1: the output capacitance of the device (known);

g_3: the real load resistance, and

g_2: the compensating element inductance.

In normalized form, we can express these quantities as:

$$g_1 = \frac{\sqrt{2}}{\gamma}$$

$$g_2 = \frac{\sqrt{2}\gamma}{1+\gamma^2}$$

$$g_3 = \frac{g_0\gamma^2}{1+\gamma^2}$$

where γ is an intermediate quantity (mathematically related to the maximum VSWR in the pass-band) used to simplify the calculations.

From the above, it follows that:

$$g_2 = \frac{2g_1}{g_1^2+2}$$

In general, $g_1 << 1$, so $\gamma >> 1$ and as a result, $g_3 \sim g_0$.

(De)normalization can be done using:

$g_0 = R$

$g_1 = \omega CR$

$g_2 = \omega L/R$

where: ω is the *maximum* angular frequency, and the maximum VSWR is g_0/g_3.

In the example with the BLF177:

$g_1 = 1/4$

$g_2 = 0.2424$ (normalized value), so L = 8.61 nH.

Therefore, the VSWR is 1.031 - a substantial improvement. And though not necessary in this case, it can be made better still as required in driver stages for which compensation with two elements, see Fig.3-21, is preferred.

Two-element compensation

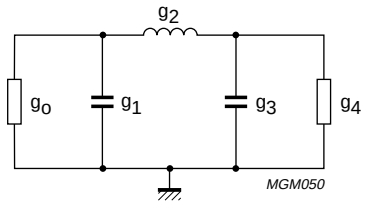


Fig.3-21 Output capacitance compensation using two elements.

The calculation is similar to that just described, so in normalized form:

$g_0 = g_4$

$$g_1 = g_3 = \frac{1}{\gamma}$$

$$g_2 = \frac{2\gamma}{\gamma^2+\frac{3}{4}}$$

From this, it follows that:

$$g_2 = \frac{8g_1}{3g_1^2+4}$$

Normalization and denormalization is done using:

$g_0 = g_4 = R$

$g_1 = g_3 = \omega CR$

$g_2 = \omega L/R$

where ω is again the *maximum* angular frequency.

The maximum VSWR is calculated as follows. For the calculation, it is necessary to introduce a term k where:

$k = \gamma + \sqrt{(\gamma^2 + 1)}$

Then:

$$VSWR = \left(\frac{k^3 + 1}{k^3 - 1}\right)^2$$

In the example with the BLF177:

$g_1 = 1/4$

$\gamma = 4$

$g_2 = 0.4776$ (so L = 17 nH)

Therefore, the VSWR = 1.007.

This is principally the same as the HF compensation of a conventional transformer. The only difference is that in the latter case the stray inductance is known and the compensation capacitors have to be calculated.

Compensation of parallel inductances

COMPENSATING ONE PARALLEL INDUCTANCE

It is also worthwhile compensating for the parallel inductances of the RF choke and output transformer found in most amplifiers as their reactances at 1.6 MHz are often about four times the load resistance. In most cases, compensation is provided by the coupling capacitor(s).

There are also simpler situations where either the RF choke or the impedance transformer is missing. We will start with this case and the equivalent circuit is given in Fig.3-22.

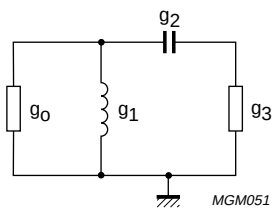


Fig.3-22 Compensation of an RF choke.

This circuit looks much the same as the HF compensation scheme, with the L and the C interchanged. Mathematically, there is also much in common - only the normalized values have to be inverted. So, for the reactive elements:

$$g_1 = \frac{\gamma}{\sqrt{2}}$$

$$g_2 = \frac{1 + \gamma^2}{\sqrt{2}\gamma}$$

$$g_3 = \frac{g_0\gamma^2}{1 + \gamma^2}$$

From these, it follows that:

$$g_2 = \frac{1 + 2g_1^2}{2g_1}$$

In general, g_1 and γ are >>1, so $g_3 \sim g_0$.

Normalization and denormalization are done using:

$g_0 = R$

$g_1 = \omega L/R$

$g_2 = \omega CR$

where ω is the *minimum* angular frequency, and the maximum VSWR is again g_0/g_3.

COMPENSATING TWO PARALLEL INDUCTANCES

If we have to compensate two parallel inductances of approximately equal value, the equivalent circuit is as shown in Fig.3-23.

Inverting the normalized values for the reactive elements gives:

$g_0 = g_4$

$g_1 = g_3 = \gamma$

$$g_2 = \frac{\gamma^2 + \frac{3}{4}}{2\gamma}$$

From these, it follows that:

$$g_2 = \frac{4g_1^2 + 3}{8g_1}$$

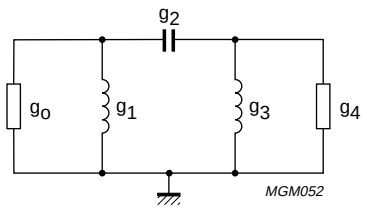


Fig.3-23 Compensation of an RF choke and impedance transformer.

Normalization and denormalization is done using:

$g_0 = g_4 = R$

$g_1 = g_3 = \omega L/R$

$g_2 = \omega CR$

where ω is the *minimum* angular frequency and the maximum VSWR is determined in the same way as in the HF situation. So, if $k = \gamma + \sqrt{(\gamma^2 + 1)}$ as defined earlier:

$$VSWR = \left(\frac{k^3 + 1}{k^3 - 1}\right)^2$$

In the example with a BLF177:

$g_1 = 4$

$\gamma = 4$

$g_2 = 2.094$

Therefore, the VSWR = 1.007

For R = 6.25 Ω and f = 1.6 MHz, we get C = 33 nF.

3.2.2.1.2 COMPENSATION AT THE INPUT

For bipolar transistors, the variations in power gain and input impedance can be compensated with an R-L-C network as decribed in application report *"AN98030"*, and shown in Fig.3-24. The network was designed using a circuit analysis program with an optimization facility.

For MOS transistors, the behaviour of the input impedance is quite different. The main problem here is providing a constant voltage across a rather high input capacitance (for the BLF177: about 745 pF) over the frequency range. At the same time, we want good matching at the input *and* the highest power gain.

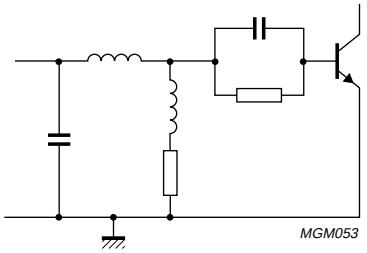


Fig.3-24 Compensation circuit of a bipolar transistor input. An example is given in report *"AN98030"*.

Simply connecting a resistor across the transistor input does not produce good results. Better solutions, the simplest of which is described here (see Fig.3-25), are required. The more advanced ones will be discussed later where their superior performance is really needed.

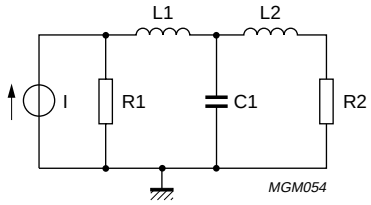


Fig.3-25 Circuit providing simple input compensation of a MOS transistor.

In Fig.3-25, the (transformed) driving generator is represented by the combination I-R_1, and the input capacitance of the transistor by C_1. The compensation components are: L_1, L_2 and R_2. R_2 should approximately equal R_1. In addition, the voltage across C_1 should not differ much from that across R_1. As the required voltage across C_1 is a given quantity, we shall design a circuit with the highest possible value of R_1 to obtain the lowest possible drive power.

Computer optimization programs can be used to investigate what happens when the product R_1C_1 is increased. The aims of optimization are to:

– Minimize the input VSWR over the frequency band, and

– Minimize the variation of the voltage across C_1 over the same band.

Table 3-2 gives the normalized results from such a program.

Table 3-2 Effect of varying $\omega C_1 R_1$ in the compensation circuit of Fig.3-25

$\omega C_1 R_1$	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG(dB)
0.8	0.437	0.305	0.961	1.21	0.19
1.0	0.515	0.388	0.939	1.34	0.31
1.2	0.571	0.473	0.908	1.51	0.44
1.4	0.619	0.568	0.867	1.74	0.64

ω is the maximum angular frequency, and ΔG the maximum deviation from the average gain.

From Table 3-2, clearly, a good practical choice is $\omega C_1 R_1 = 1.0$. For the BLF177, this means that R_1 can be 7.6 Ω maximum. For ease of transformation, we chose 6.25 Ω.

The input impedance of the transistor is not of course a pure capacitance. It also has some series resistance and inductance, so reoptimization is necessary to take account of the real input impedance and power gain of the transistor as a function of frequency.

For driver stages operating at a low power level, negative feedback is sometimes used: an emitter resistor and a collector-base resistor for bipolar devices (with in some cases an inductance in series with the latter to reduce feedback at the high end of the frequency band).

Similarly, for MOS transistors, a resistor is connected between drain and gate. A resistor is not required in the source lead however. The advantage of this feedback method is lower intermodulation distortion. The feedback must not be too large however as such a resistor consumes part (albeit a small part) of the output power.

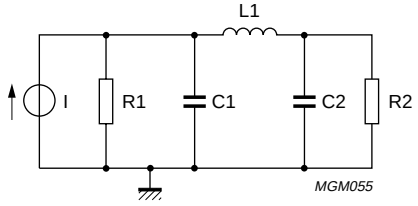


Fig.3-26 Equivalent circuit of output compensation for the lower VHF range.

3.2.2.2 THE LOWER VHF RANGE

WIDEBAND VHF MATCHING CIRCUITS OVERVIEW

Lower VHF range *(Section 3.2.2.2)*

– Though the same circuit configurations used for HF can be used in this range, the higher maximum frequency requires modified component values.
– *Section 3.2.2.2.1* describes two circuits that compensate for output capacitance.
– *Section 3.2.2.2.2* describes two input networks using more compensation elements than the HF version for higher power gain.

Upper VHF range *(Section 3.2.2.3)*

– Describes impedance matching (input and output) for this range using low-pass L-sections, with an optional high-pass section.
– *Section 3.2.2.3.1* describes a single low-pass section, sufficient for low impedance ratios and/or moderate bandwidths. To meet more stringent requirements, two or three sections are required. *Section 3.2.2.3.2* outlines several approaches, some suitable for interstage networks.
– Finally, the effect of non-ideal network components is discussed.

Some military communications transmitters operate in this range. The lowest frequencies used are 25 to 30 MHz and the highest 90 to 110 MHz.

Power amplifiers for this range are similar to those for the HF range. However, impedance matching can only be done with transmission line transformers as described in application report *"ECO7703"*. In addition, more complex methods are required for RF compensation at both output and input.

3.2.2.2.1 COMPENSATION AT THE OUTPUT

The output compensation systems described in Section 3.2.2.1.1 provide adequate results in the HF range. For the lower VHF range, somewhat better results can be obtained simply by modifying the component values. The equivalent circuit is shown in Fig.3-26.

First, let $R_1 = R_2$; C_2 does not however have to equal C_1. Computer optimization for lower VHF yields the results shown in Table 3-3.

The practical limit of usefulness is at $\omega C_1R_1 = 1.0$. If we use this condition with the Chebyshev system described earlier, then the maximum VSWR would be 1.33 instead of 1.29.

Table 3-3 Computer optimization results of the compensation circuit of Fig.3-26 for the lower VHF range

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	$VSWR_{max}$
0.6	0.549	0.914	1.08
0.8	0.693	1.04	1.17
1.0	0.827	1.10	1.29
1.2	0.965	1.12	1.44

ω is the maximum angular frequency. $R_1 = R_2$.

With this compensation, we can go one step further by dropping the requirement that R_2 has to equal R_1. Doing this and optimizing again yields the results shown in Table 3-4.

As Table 3-4 shows, for $\omega C_1R_1 = 1.0$, the maximum VSWR is improved to 1.25, and the corresponding value of R_2 is now smaller than R_1. Whether this is an advantage or not is difficult to say as it is dependent on the desired combination of supply voltage and output power as well as on the possible transformer ratios.

Table 3-4 Computer optimization results of the compensation circuit of Fig.3-26 for the lower VHF range. $R_1 \neq R_2$

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	R_2/R_1	$VSWR_{max}$
0.6	0.468	0.818	0.939	1.08
0.8	0.615	0.922	0.897	1.16
1.0	0.738	0.943	0.838	1.25
1.2	0.886	0.943	0.783	1.36

ω is the maximum angular frequency, and $R_1 \neq R_2$.

3.2.2.2.2 INPUT NETWORKS

For bipolar transistors, it should be possible to use the same type of compensation network used for the HF range in the lower VHF range. However, we shall restrict our considerations to input networks for use with MOS devices.

The problem is the same as for the HF range (maintaining a constant voltage across a capacitance over a wide frequency range, see Section 3.2.2.1.2), but with a substantially higher maximum frequency. So, a more efficient compensation network is needed, requiring more components. The first of two examples is shown in Fig.3-27.

C_2 represents the input capacitance of the transistor. The results obtained by computer optimization are shown in Table 3-5.

Compared with the network described earlier (Fig.3-25 and Table 3-2), there is substantial improvement because ωR_1C_2 can certainly be increased up to 1.6, compared with 1.0 for the simpler network, providing higher gain for a given bandwidth.

A second circuit configuration producing as good or even superior results is shown in Fig.3-28. Here, the input capacitance of the transistor is represented by C_1. Computer optimization yields the results summarized in Table 3-6.

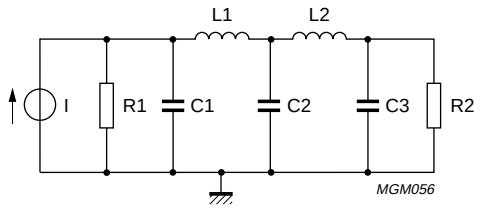


Fig.3-27 Example of an improved compensation circuit for the lower VHF range.

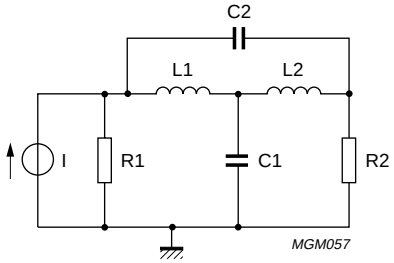


Fig.3-28 Second example of an improved compensation circuit for the lower VHF range.

Table 3-5 Computer optimization results of the compensation circuit of Fig.3-27

ωR_1C_2	ωR_1C_1	ωR_1C_3	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG (dB)
1.0	0.460	0.501	0.870	0.836	1.02	1.10	0.10
1.2	0.602	0.496	1.02	0.836	1.00	1.14	0.15
1.4	0.751	0.485	1.11	0.836	0.977	1.21	0.20
1.6	0.887	0.476	1.15	0.845	0.955	1.31	0.28
1.8	0.993	0.482	1.15	0.870	0.934	1.42	0.38

ω is the maximum angular frequency and ΔG the maximum deviation from the average gain.

Table 3-6 Computer optimization results of the compensation circuit of Fig.3-28

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG (dB)
1.0	0.591	0.392	0.336	0.977	1.12	0.11
1.2	0.597	0.447	0.396	0.972	1.15	0.13
1.4	0.604	0.504	0.462	0.966	1.19	0.16
1.6	0.584	0.584	0.536	0.961	1.21	0.18
1.8	0.584	0.662	0.611	0.955	1.23	0.20
2.0	0.574	0.794	0.733	0.934	1.21	0.36

ω is the maximum angular frequency and ΔG the maximum deviation from the average gain.

Comparing these results with those of the previous case, we see that the product ωC_1R_1 can be increased to 1.8 and possibly to 2.0. So, this configuration, even though it uses one component fewer, is better. Experience shows that circuits using inductive coupling between L_1 and L_2 do not improve the VSWR and gain variation performance.

As mentioned earlier, the input impedance of a MOS transistor can be represented by a capacitance, inductance and resistance in series. At high power levels in particular, the resistance cannot be neglected.

As a guideline, reoptimization is necessary when the values of input VSWR and gain variation are inferior to those in Tables 3-2, 3-5 and 3-6.

3.2.2.3 THE UPPER VHF RANGE

To get an idea of the impedance levels in this frequency range, consider a BLF225 MOS transistor able to deliver 30 W at 175 MHz from a 12.5 V supply voltage (Note, bipolar devices for the same range have similar impedance levels).

Suppose that the BLF225 is used in a mobile radio transmitter for the range 132 to 174 MHz. The optimum load impedance is about 2.5 Ω with a rather small reactive component. At the transistor input, there is an effective capacitance of 215 pF in series with a resistance of 3.2 Ω and a small inductance of 0.21 nH.

In the literature, most networks for wideband impedance matching are based on pure resistances. So, we have to start by making the impedance at the input approximately real. In theory, this can be done with either a parallel or a series inductance. Though the former should be preferable as it provides a higher impedance, unfortunately, a small inductance in parallel with the input of a transistor can cause large parasitic oscillations. Therefore, we have to use a series inductance, giving a tuned circuit with a loaded Q-factor of 1.53 in the middle of the frequency band. The relative width of this band ($\Delta f/f_0$) is 27 to 28% . If the product of loaded Q-factor and relative bandwidth is much less than 1, as in this case, the matching will not be affected significantly.

The remaining task is to match resistances of 3.2 Ω and 2.5 Ω to a 50 Ω source and load over the range 132 to 174 MHz. The most popular type of network for this purpose comes from G.L. Matthaei (Ref.2) where the matching is obtained from one or more low-pass L-sections (the more sections, the lower the VSWR in the pass-band).

The essence of this method is that there are several frequencies in the pass-band at which exact matching occurs. The number of exact matches is equal to the number of sections.

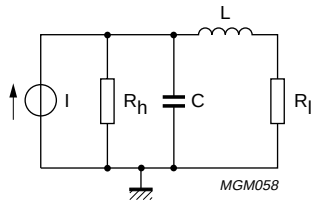


Fig.3-29 Single-section matching network for the upper VHF range.

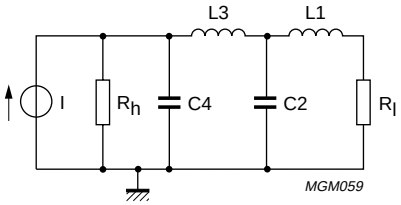


Fig.3-30 Two-section matching network for the upper VHF range.

3.2.2.3.1 SINGLE-SECTION MATCHING

First consider when there is just one section, Fig.3-29. R_h is the higher of the two resistances and R_l the lower. Exact matching takes place at:

$$f_0 = \sqrt{\frac{1}{2}\left(f_l^2 + f_h^2\right)}$$

where f_l is the lower limit of the band and f_h the upper one.

L and C can be calculated in the same way as described in Section 3.2.1.1. The maximum VSWR in the pass-band follows from the input impedance at one of the band limits.

The results of the calculation for the output, where 2.5 Ω must be matched to 50 Ω, are:

f_0 = 154.4 MHz

L = 11.23 nH

C = 89.84 pF

VSWR = 2.974.

The VSWR calculation is rather complex and is best done using a circuit analysis program. The high VSWR obtained here indicates that one section is not sufficient. Therefore, we shall now consider some possibilities with two sections.

3.2.2.3.2 TWO-SECTION MATCHING

Two low-pass sections

If both sections are low-pass, the situation is as shown in Fig.3-30.

Exact matching takes place at f_1 and f_2 ($f_2 > f_1$) and:

$$f_1 = \frac{1}{2}\sqrt{(2+\sqrt{2})\,f_l^2 + (2-\sqrt{2})\,f_h^2} \quad \text{and}$$

$$f_2 = \frac{1}{2}\sqrt{(2-\sqrt{2})\,f_l^2 + (2+\sqrt{2})\,f_h^2}$$

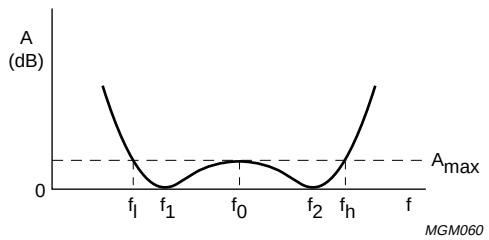


Fig.3-31 Pass-band characteristic of the two-section matching circuit of Fig.3-30.

There is maximum attenuation at the band limits, but also at:

$$f_0 = \sqrt{\frac{1}{2}\left(f_l^2 + f_h^2\right)}$$

The pass-band characteristic is shown in Fig.3-31.

To determine the values of the components, we need to define an auxiliary quantity M where:

$$M = L_1 C_2 = \frac{\sqrt{1 - \frac{R_h}{R_l}}}{\omega_1 \omega_2}$$

in which $\omega_1 = 2\pi f_1$
and $\omega_2 = 2\pi f_2$.

Then, for the circuit of Fig.3-30:

$$L_1 = \sqrt{\frac{-p}{2} + \sqrt{\frac{p^2}{4} - q}}$$

where:

$p = -R_l \{MR_h(\omega_1^2 M - 2) + (R_h - R_l)/\omega_1^2\}$, and

$q = -M^2 R_l^3 R_h$

And, for the other components:

$C_2 = M/L_1$

$L_3 = C_2 R_l R_h$

$C_4 = L_1/(R_l R_h)$.

To calculate the maximum VSWR in the pass-band, the procedure used for single-section matching must again be followed.

For this example, where we need to match from 2.5 to 50 Ω in the frequency range 132 to 174 MHz, we obtain:

f_1 = 138.9 MHz C_2 = 197.4 pF

f_2 = 168.5 MHz L_3 = 24.67 nH

L_1 = 5.343 nH C_4 = 42.74 pF

The maximum VSWR (from the circuit analysis program) in the pass-band is now 1.173, which is a far better result than with one section (2.974).

Though the calculation procedure described above is rather complicated, direct use of the Matthaei method (Ref.2) is not simple either because:

– Interpolation is required both for impedance ratio and relative bandwidth
– Denormalization must be used, and
– Insertion loss must be converted to VSWR.

One low-pass and one high-pass section

Another method of wideband impedance matching is described by U. Fleischmann. (Refs 3, 4 and 5). In this method, two L-sections are used: one low-pass, the other high-pass. Both sequences are possible, and the resulting pass-band characteristic is almost equal to that of the previous case with two sections. To simplify calculation, we need to define several quantities:

$$f_0 = \sqrt{f_l f_h}$$

where f_l and f_h are the lower and upper limits of the frequency band respectively.

$$d = \frac{f_h - f_l}{f_0}$$

$$m = \frac{R_h}{R_l}$$

$$\varepsilon = \frac{-d^2\sqrt{m}}{4} + \sqrt{\left(\frac{d^2\sqrt{m}}{4}\right)^2 + \left(\frac{d^2+2}{2}\right)}, \text{ and}$$

$k = \varepsilon\sqrt{m}$.

Now we are able to calculate the normalized component values, first for when the low-pass section is adjacent to the lower resistance, R_l, see Fig.3-32.

LOW-PASS SECTION NEAR R_l

In this case:

$$g_1 = \frac{1}{k}\sqrt{\frac{k-1}{m}}$$

$$g_2 = \sqrt{m(k-1)}$$

$$g_3 = \sqrt{\frac{m}{k-1}}$$

$$g_4 = \frac{k}{\sqrt{m(k-1)}}$$

Denormalization can be done for each element using:

$g = \omega_0 L/R_h$ and

$g = \omega_0 C R_h$

where $\omega_0 = 2\pi f_0$

Then, the maximum VSWR in the pass-band becomes:

$VSWR = 1/\varepsilon^2$

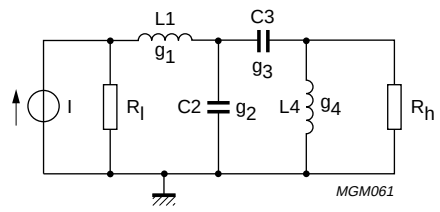


Fig.3-32 Two-section matching network using two L-sections.

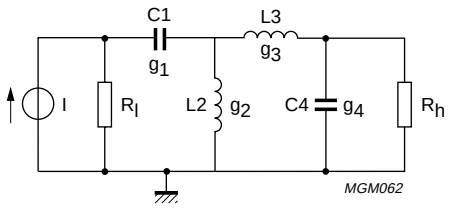


Fig.3-33 Two-section matching network using two L-sections (section sequence reversed compared with that in Fig.3-32).

LOW-PASS SECTION NEAR R_H

If the sequence of the sections is now reversed, the situation is as in Fig.3-33.

In this case, the normalized element values have to be inverted, so:

$$g_1 = k\sqrt{\frac{m}{k-1}}$$

$$g_2 = \frac{1}{\sqrt{m(k-1)}}$$

$$g_3 = \sqrt{\frac{k-1}{m}}$$

$$g_4 = \frac{1}{k}\sqrt{m(k-1)}$$

Denormalization is done as in the previous case, and the maximum VSWR remains the same ($1/\varepsilon^2$).

To match 2.5 to 50 Ω over 132 to 174 MHz, (see Section 3.2.2.3.2), the calculation gives the following results:

1st case (circuit as in Fig.3-32):

L_1 = 5.005 nH ; C_2 = 167.7 pF

C_3 = 52.6 pF ; L_4 = 27.54 nH

2nd case (circuit as in Fig.3-33):

C_1 = 220.3 pF ; L_2 = 6.575 nH

L_3 = 20.97 nH ; C_4 = 40.04 pF.

VSWR (both cases) = 1.14

The results are slightly better than those obtained with two low-pass sections. Other advantages are:

– Easier calculation

– Useful for interstage networks.

A disadvantage is the reduced suppression of harmonics.

Effect of real ('imperfect') components on the calculations

When implementing these wideband networks, keep in mind that capacitors, even surface-mount (chip) capacitors, are not ideal components. A chip capacitor, for example, has a series inductance of about 1 nH. In the example with two low-pass sections, a capacitance of 197 pF was required. If two capacitors in parallel are used, their combined inductance is 0.5 nH. As a consequence, we have to reduce the capacitance to C' where:

$$C' = \frac{C}{\omega^2 LC + 1}$$

Note, ω is the average angular frequency of the band, so in the example:

$$C' = \frac{197}{1.09} = 181 \text{ pF}$$

3.2.2.4 THE LOWER UHF RANGE

For the lower UHF range, the methods used in the upper VHF range can again be employed. However, it is not always very practical to use discrete inductances because of the very low values required, and these should then be replaced by striplines.

Note that a stripline is not a pure series inductance; it has parallel capacitance which must be taken into account in any network design. In addition, a particular inductance can be obtained with striplines of different characteristic resistance, R_c. Wherever, possible, use striplines with relatively high R_c as they generally have lower parallel capacitances.

If a transmission line is shorter than 1/8th of a wavelength, a good approximation is the LC equivalent circuit shown in Fig.3-34 where:

$L = R_c l/v$

$C = l/R_c v$

where $v = 3\text{x}10^8/\sqrt{\varepsilon_r}$. ($\varepsilon_r$ being the *effective* relative dielectric constant of the print board).

What was said about the parasitic inductance of real capacitors at VHF frequencies is of course even more relevant at UHF frequencies.

WIDEBAND UHF MATCHING CIRCUITS OVERVIEW

Lower UHF range *(Section 3.2.2.4)*

– In this range, the techniques used in the upper VHF range can again be used. The main difference is the more frequent use of striplines. In Section 3.2.2.4, the equivalence between striplines and LC-networks is given.

Upper UHF range *(Section 3.2.2.5)*

– This section outlines the considerations for very wide bandwidths (about 1 octave).

– *Section 3.2.2.5.1* covers the use of band-pass networks for the output circuit. These are based on an equivalent low-pass circuit and contain one or two Norton transformations (inductive and capacitive) including T and Pi equivalents.

– Input networks for this range are usually designed for the highest possible flat power gain, and often have a poor input VSWR at the lower end of the range. To improve performance, two identical amplifiers can be combined with 3 dB 90° hybrid couplers as outlined in *Section 3.2.2.5.2.* Constructing couplers for less-demanding applications is also described, as is the design procedure for the input matching network.

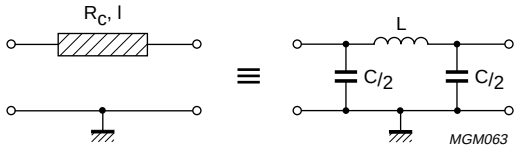


Fig.3-34 LC equivalent circuit of a transmission line shorter than 1/8th of a wavelength.

3.2.2.5 THE UPPER UHF RANGE

Here, we shall consider wideband circuits for TV bands IV and V, covering 470 to 860 MHz, i.e. a bandwidth of 390 MHz.

In Section 3.2.2.3 (Upper VHF range), we described how to match two widely different resistances over a wide range of frequencies. For two pure resistances, matching is always possible, though more sections are required as the resistance ratio and/or the relative bandwidth increases.

Now consider when one or both impedances have a large reactive component - a parallel-RC combination, or a series-RL circuit. In both cases, a time constant, τ, is involved: τ = RC or L/R.

According to Bode (see also Refs 6 and 7), there is a limit to the reflection coefficient, r, which can be achieved in the pass-band. This limit depends on the time constant and the required (absolute) bandwidth, even when the number of elements in the matching network is made arbitrarily high and is:

$$\int_0^\infty \ln\left|\frac{1}{r}\right| d\omega = \frac{\pi}{\tau}$$

If we assume that r is constant in the pass-band, and equal to one in the stop-bands, this relation can be simplified to:

$$2\pi B\tau = \pi / \ln\left|\frac{1}{r}\right|$$

where B is the absolute bandwidth.

This relationship is shown in Fig.3-35.

According to Bode, the area below the curve is given by the time constant. If r is less than 1 in the stop-bands, and varies in the pass-band, then the maximum value of r in the pass-band will be higher than the theoretical value.

For example, suppose the maximum acceptable VSWR in the pass-band is 1.25, then r = 0.111. For the ideal case, this gives: $2\pi B\tau = 1.43$; in practice, $2\pi B\tau$ will rarely exceed 1.0, and then only by a very small amount.

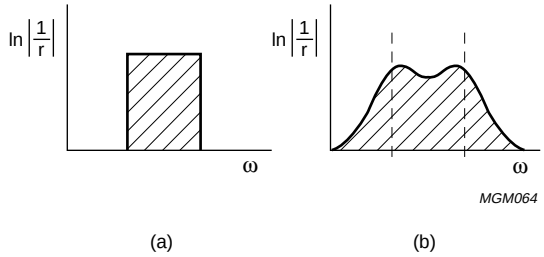


Fig.3-35 (a) Ideal and (b) practical plot of $\ln\left|\frac{1}{r}\right|$ as a function of ω (i.e. 2π times the frequency).

3.2.2.5.1 OUTPUT NETWORKS

As an example, take the BLW98, a class-A TV-transposer transistor for bands IV/V (bandwidth, B = 390 MHz). At V_{CE} = 25 V and I_C = 0.85 A, a BLW98 is able to deliver about 4 W peak sync power with a 3-tone intermodulation distortion of –60 dB. Under these conditions, the effective output capacitance, C_C, is ~20 pF, and the optimum load resistance in class-A operation is ~20 Ω. So the time constant, τ, of the transistor output is ~400 ps, and $2\pi B\tau$ then becomes 0.98, meaning that the required bandwidth can just be realized without serious concessions in output power and IMD in parts of the frequency band.

The equivalent output circuit of a transistor without internal output matching is shown in Fig.3-36.

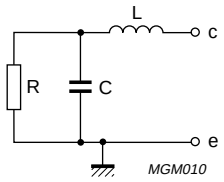


Fig.3-36 Equivalent circuit of the output of a transistor without internal output matching.

The values of R, C and L can be derived from the published curves for optimum load impedance versus frequency. Here, computer programs for circuit analysis with an optimization facility can be very helpful. A good approximation however can also be made using the following:

R: In class-A amplifiers, $R = NV_{CE}/I_C$ where $N = 0.65$ to 0.80. In other classes, $R = V_C^2/(2P_o)$ but note that for linear class-AB amplifiers, V_C must be chosen 10 to 15% below the supply voltage.

C: In the HF and VHF range, $C = NC_C$ where $N = 1.10$ to 1.15. In the UHF range (especially in the upper part), higher efficiency and gain can be obtained when the output capacitance is not completely tuned out. In practice, an amount $\Delta C = 0.5/(\omega_m R)$ may be subtracted where ω_m is the maximum angular frequency of the band.

L: This is approximately $L_c + L_e/2$ (about 1 to 2 nH in practice) where L_c and L_e are respectively the collector and emitter self-inductance.

The next step is to choose the configuration of the matching network. Where a large bandwidth is required, as in this example, it can be a big advantage to make the collector RF choke part of the matching network. This can be arranged in two ways. The simplest is where the collector RF choke tunes out the imaginary part of the output impedance in the middle of the band. A better and theoretically more correct method is to apply a Norton transformation as shown in Fig.3-37.

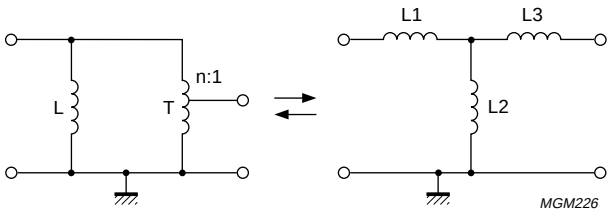


Fig.3-37 Norton transformation.

T is an ideal transformer which transforms the voltage down by a factor n (n > 1). 'Ideal' means the transformer has no parallel and no stray inductance, i.e. there is 100% coupling between the windings.

The other quantities are:

$$L_1 = L\left(1 - \frac{1}{n}\right)$$

$$L_2 = \frac{L}{n}$$

$$L_3 = \frac{-L\,(n-1)}{n^2}$$

Note, L_3 is negative but this is subsequently 'absorbed' in the remainder of the network. $L_1 \geq L$ in the equivalent output circuit (Fig.3-36) of the transistor.

Combining Figs 3-36 and 3-37 yields Fig.3-38. So, the transistor output impedance becomes a parallel connection of R', C' and L' where:

$$R' = \frac{R}{n^2}$$

$$C' = Cn^2$$

$$L' = \frac{L}{n^2}$$

Now we can arrange that the LC-parallel circuit resonates in the middle of the frequency band. Furthermore, we can vary R' within certain limits.

At the 50 Ω side, the same kind of transformation in reverse can be made if required. In this case, a capacitive transformation is also possible, see Fig.3-39 where:

$$C_1 = \frac{-n^2 C}{n-1}$$

$$C_2 = nC$$

$$C_3 = \frac{nC}{n-1}$$

Here, C_1 is negative and so it has also to be absorbed in the remainder of the network.

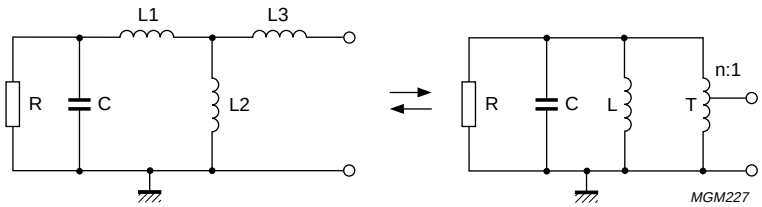


Fig.3-38 Norton transformation at transistor output.

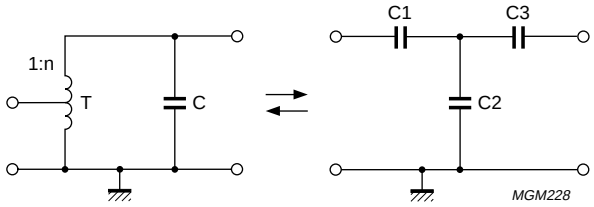


Fig.3-39 Alternative transformation at 50 Ω load side.

Sometimes a Pi-equivalent is needed instead of a T-equivalent. This can be obtained as indicated in Fig.3-40 for the capacitive case where:

$$B_{12} = \frac{B}{n}$$

$$B_{20} = B\left(1 - \frac{1}{n}\right)$$

$$B_{10} = \frac{-B\,(n-1)}{n^2}$$

This transformation also has an inductive equivalent in which $B = -1/\omega L$ instead of ωC.

Now we return to Fig.3-38 to complete the impedance matching. Several methods are possible:

– The Matthaei method as described in Section 3.2.2.3.2
– The Fleischmann method as described in Section 3.2.2.3.2
– A band-pass network as depicted in Fig.3-41.

The network of Fig.3-41 can only be used if R_1 does not differ too much from R_3, say $2R_3 \geq R_1 \geq R_3/2$. If so, we can apply the Norton transformation (just discussed) at the input and, if necessary, also at the output.

This band-pass network has been derived from an equivalent low-pass Chebyshev filter as shown in Fig.3-42.

Components with the same identifiers (in Figs 3-41 and 3-42) have the same values. Components L_1, C_2 and L_3, added in the band-pass network, resonate with the parallel or series-connected components at the geometric mean frequency of the passband, f_0:

$$f_0 = \sqrt{f_1 f_2}$$

where f_1 and f_2 are the lower and upper limits of the pass-band respectively.

L_1 resonates with C_1; C_2 resonates with L_2, and L_3 resonates with C_3

In Fig.3-42, without a Norton transformation:

$R_1 = R_3$

$C_1 = C_3$.

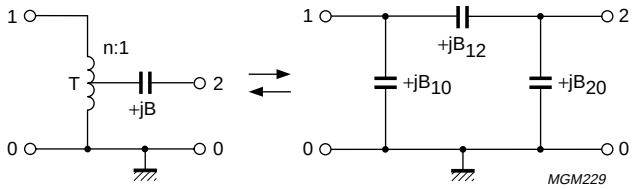


Fig.3-40 Norton transformation with Pi equivalent.

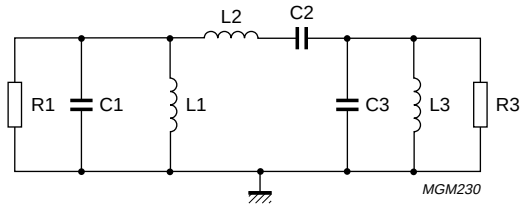


Fig.3-41 Band-pass network for output matching.

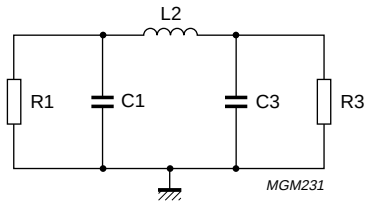


Fig.3-42 Low-pass network equivalent to Fig.3-41.

By combining some equations from the two-element compensation of Section 3.2.2.1.1, we can express L_2 as:

$$L_2 = \frac{8R_1^2C_1}{3(\omega C_1 R_1)^2 + 4}$$

where ω is 2π times the required bandwidth. The maximum VSWR of this network can be calculated in the same way as in Section 3.2.2.1.1 where:

$$\gamma = \frac{1}{\omega R_1 C_1}$$

and

$$k = \gamma + \sqrt{\gamma^2 + 1}$$

from which

$$VSWR = \left(\frac{k^3 + 1}{k^3 - 1}\right)^2$$

Since the Norton transformation does not change the product R_1C_1, this product is the same as that of the equivalent circuit of the transistor output (Fig.3-36). A circuit like that of Fig.3-41, plus transformations, has been made for the BLW32 with R = 82 Ω and C = 4.2 pF. With a bandwidth of 390 MHz this gives:

$\omega RC = 0.8439$

$\gamma = 1.185$

$k = 2.735$

VSWR = 1.216.

This is very acceptable performance. In practice. the inductances are replaced by striplines as described in Section 3.2.2.4. Re-optimization is then required and the final VSWR will be somewhat higher because of the capacitance of the striplines and the inductance of the SMD chip capacitors. See also application report *"ECO7806"*.

If the Matthaei or Fleischmann method is used instead of the one above, note that:

– For TV band IV/V, three sections (instead of two) may be necessary

– Besides several low-pass elements, sufficient high-pass elements are used. The former are the series inductances and parallel capacitances; the latter are the parallel inductances and series capacitances.

This is necessary to meet, as far as possible, the conditions for the lowest possible reflection coefficient in the pass-band according to the Bode integral. So, three low-pass sections are not as good as two low-pass plus one high-pass section.

3.2.2.5.2 INPUT NETWORKS

What is desired at the input is a network that gives good impedance matching over the entire frequency band while compensating for the variations in transistor gain with frequency. The overall gain (transistor plus network) should be roughly equal to the transistor gain at the highest frequency of the band.

For low powers, as in driver stages, this can be realized with a network containing one or two resistors. For high powers, there are better solutions, namely:

1. Make a network giving good impedance matching over the frequency band, and compensate the gain variation somewhere else in the amplifier chain or,
2. Make a network giving an (almost) exact match at the highest frequency of the pass-band and increasing mismatch at lower frequencies such that the increasing gain of the transistor is compensated in the best possible way.

The second approach is much easier to realize because the loaded Q-factors in the network may be higher than with the first approach.

Assuming a gain variation of the transistor of 6 dB per octave, the input VSWR at the lowest frequency of TV bands IV and V will be 11.3 if the second method is followed. Clearly, the preceding amplifier stage cannot function normally under these conditions. Fortunately, there is a simple solution to this problem - make two identical amplifier stages according to this principle and combine them with 3 dB, 90° hybrid couplers as shown in Fig.3-43.

The first hybrid coupler splits the drive power delivered at port 1 into two equal parts at ports 2 and 3, and introduces a 90° phase shift between the two signals. If ports 2 and 3 are loaded with 50 Ω, the output at port 4 is zero.

The most important property of a 90° hybrid coupler is that equal amounts of mismatch at ports 2 and 3 do not influence the matching at port 1; any reflected power goes to port 4. The mismatch at ports 2 and 3 must however be equal in amplitude and phase.

At the second coupler, the opposite happens. For two input signals of equal amplitude and 90° phase difference, the output is the sum of the powers while the power at port 4 is again zero. If the powers are not equal or the phase difference deviates from 90°, then the power difference appears on port 4.

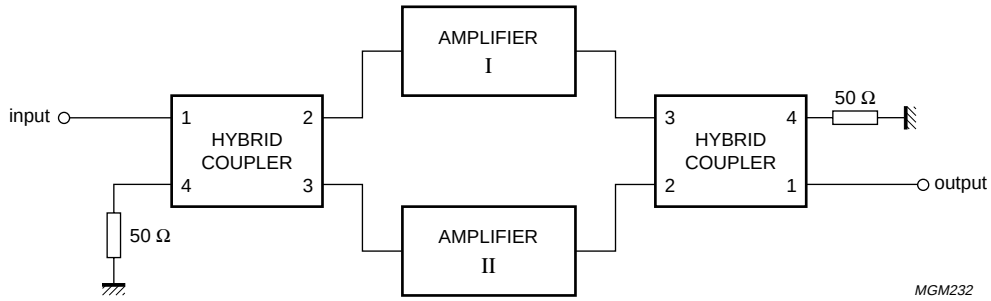


Fig.3-43 Input/output network using two identical amplifiers and 90° hybrid couplers to lower VSWR.

This sort of hybrid coupler with a full octave bandwidth and continuous power handling of 200 W is available from Anaren, USA.

Another American company, Sage, delivers the Wireline. This is a special semi-rigid coaxial cable with two inner conductors. A hybrid coupler is formed from a 1/4 λ cable for the middle of the frequency band. Note, the wavelength in this cable is about two-thirds that in free space. The Wireline is available in several thicknesses to suit different power requirements. For high powers, another product with a square cross-section is available (Wirepack).

If the bandwidth requirements are less severe, 90° hybrid couplers can be made from striplines as shown in Fig.3-44. Here, four striplines of 1/4 λ and characteristic resistances of 50 and 35.4 Ω are used. In a practical implementation, it is usual to:

– Replace the striplines by LC equivalents see Fig.3-45, or
– Make the hybrid coupler with shortened striplines, and add compensation (multilayer SMD) capacitors, see Fig.3-46.

In Fig.3-46, let tan βl = t then:

$$R'_c = R_c\sqrt{\frac{1+t^2}{t^2}}$$

$$X_c = R_c\sqrt{1+t^2}$$

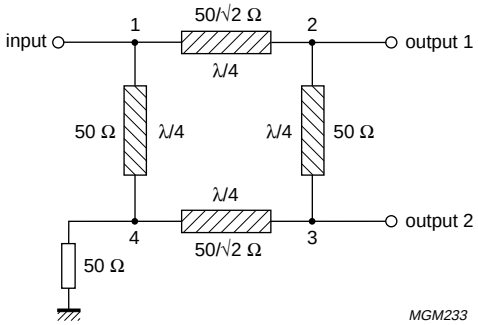


Fig.3-44 90° hybrid coupler based on striplines.

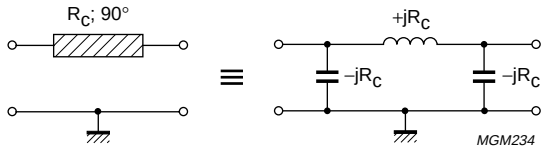


Fig.3-45 LC equivalent of a stripline.

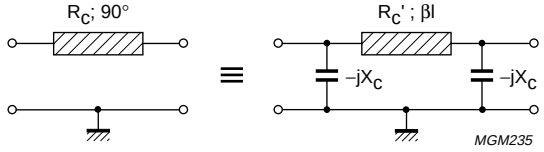


Fig.3-46 Shorter stripline equivalent using compensation capacitors.

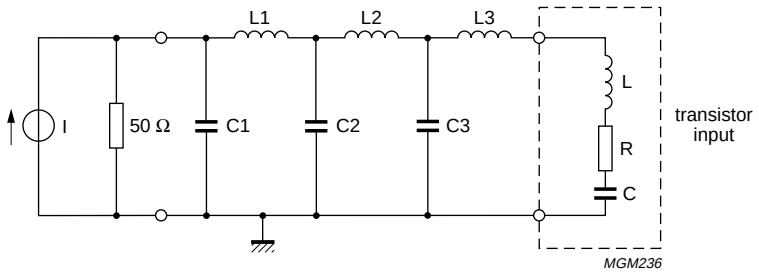


Fig.3-47 Typical input matching network.

Procedure for designing an input matching network

When calculating input matching networks, it is useful to know the RLC series-equivalent of the transistor input impedance. A first estimate can be made on the basis of the published graph of input impedance versus frequency. More accurate estimates can be obtained with the aid of a circuit analysis computer program.

To design an input matching network meeting the conditions mentioned earlier, use the following procedure, see Fig.3-47.

The last section (L_3-C_3) is designed for the highest frequency of the band. For bipolar transistors, the value of C is so high that it has no practical influence. The best value for the loaded Q-factor in this case is then about 4, and the resistance R is transformed up by a factor $Q^2 + 1$, so about 17 times.

For MOS transistors, a lower loaded Q-factor is required because of the relatively smaller value of C. A good value for Q is 2 to 3. The resistance R is then transformed up by a factor of 5 to 10, resulting in a sufficiently flat power gain.

The remaining sections, L_1-C_1 and L_2-C_2, can be calculated using the Matthaei method for the entire frequency band starting from the value found for R ($Q^2 + 1$) and the 50 Ω of the generator.

In the example above, the remaining part of the matching used two sections. In some cases, one is sufficient, but this depends on the value of R. The lower this is the more sections are required.

3.2.3 Interstage networks

Impedance matching networks between successive stages can be designed in the same way as discussed in the previous sections. For narrow-band amplifiers, this can be done directly (i.e. with no intermediate 50 Ω impedance level). However, for wideband amplifiers it is very useful to choose an intermediate impedance of 50 Ω to facilitate the alignment of the amplifier. The best way to align the output part of the network is by means of a dummy load. We shall return to this later in Section 3.5.1.

3.3 Guidelines for choosing print boards and components

3.3.1 Print board materials

Two main print board materials are used for constructing test circuits and practical RF power amplifiers: epoxy fibreglass and Teflon fibreglass.

3.3.1.1 EPOXY FIBREGLASS

The relative dielectric constant (ε_r) of this material can vary between 4 and 5; the average, 4.5, is suitable for most calculations. The material is available in several thicknesses, the most popular being: 1/16 inch (~1.6 mm) and 1/32 inch (~0.8 mm). The copper thickness commonly used is called 1 oz. which corresponds to a thickness of ~38 μm.

The dielectric loss factor of epoxy fibreglass is rather poor (tan δ = 0.030 to 0.035). This means a capacitor formed from part of the board itself has an unloaded Q-factor of only about 30, limiting this type of board to HF and VHF circuits. The board can however be used for interconnecting components and making low-impedance striplines.

Sometimes, even an interconnection area can cause problems. Take for instance point A in the circuits of Section 3.2.1.2. Suppose that the area of this connection is 1 cm^2 and the board thickness is 1.6 mm, then the capacitance will be about 3.35 pF. At 175 MHz and a Q_o of 30, the parallel resistance will therefore be 8150 Ω.

If the transistor operates at a supply voltage of 28 V say, and the coil in the matching network has a loaded Q of 5, the voltage at point A is 140 V maximum and the power loss in this connection area is approximately 1.2 W. This is already on the high side and, when the supply voltage and/or the loaded Q are higher, it can be considerably more. A good remedy in such a case is to remove the copper on the bottom side of the board beneath the connection area, and also to remove some heatsink material in the same region.

3.3.1.2 TEFLON FIBREGLASS

Another popular material is Rogers RT/duroid with an ε_r of 2.2. This material can be obtained in the same dielectric and copper thicknesses as epoxy fibreglass. The losses are considerably lower (tan δ = 0.001 to 0.002), making it very suitable for UHF circuits with striplines.

Tables 3-7 and 3-8 show the relationship between the characteristic resistance of stripline, R_c, and its width, w, for 1/16 inch and 1/32 inch board thicknesses. The table data have been generated by computer program based on information in Ref.8. The quantity SQRT ε_r is the line shortening factor by which the stripline length with air as a dielectric must be divided to obtain the line length on the print board. In addition, the inductance and capacitance per mm line length are given.

Table 3-7 Some characteristics of 1/16” (1.575 mm) Teflon fibreglass (Rogers RT-duroid)

W (mm)	**R_c** (Ω)	**SQRT** ε_r	**L/l** (nH/mm)	**C/l** (pF/mm)
4.746	50.00	1.367	0.22783	0.09113
1.000	113.23	1.313	0.49574	0.03866
1.500	95.47	1.325	0.42157	0.04625
2.000	83.15	1.334	0.36970	0.05348
2.500	73.90	1.342	0.33054	0.06052
3.000	66.64	1.349	0.29960	0.06745
3.500	60.77	1.355	0.27439	0.07431
4.000	55.90	1.360	0.25341	0.08110
4.500	51.79	1.365	0.23562	0.08785
5.000	48.28	1.369	0.22034	0.09454
5.500	45.23	1.373	0.20705	0.10120
6.000	42.57	1.377	0.19538	0.10782

ε_r = 2.200; H = 1.575 mm; Th = 0.0350 mm.

Table 3-8 Some characteristics of 1/32” (0.787 mm) Teflon fibreglass (Rogers RT-duroid)

W (mm)	**R_c** (Ω)	**SQRT** ε_r	**L/l** (nH/mm)	**C/l** (pF/mm)
2.352	50.00	1.364	0.22739	0.09095
1.000	82.31	1.330	0.36492	0.05386
1.500	66.12	1.346	0.29656	0.06783
2.000	55.53	1.357	0.25127	0.08148
2.500	48.00	1.367	0.21874	0.09493
3.000	42.36	1.375	0.19413	0.10820
3.500	37.95	1.382	0.17480	0.12135
4.000	34.42	1.388	0.15917	0.13439
4.500	31.51	1.393	0.14626	0.14733
5.000	29.07	1.397	0.13538	0.16021
5.500	26.99	1.401	0.12608	0.17302
6.000	25.21	1.405	0.11804	0.18578

ε_r = 2.200; H = 0.787 mm; Th = 0.0350 mm.

The main function of a stripline in a circuit is to provide a particular inductance. As a narrow, short line can have the same inductance as a wide, long one, see Tables 3-7 and 3-8, a choice has to be made based on power handling. The reactive power, i.e. the volt-ampere product, that the line is required to handle must be taken into account, i.e.:

$$P\beta l\,(s + 1/s)$$

where:

P is the power transferred

βl is the electrical line length in radians

s is the voltage standing wave ratio.

Dividing this product by the unloaded Q-factor of the line, (usually 200 - 400) gives the power lost in the line.

A collector or drain RF choke can also be made in the form of a stripline. The reactance of a line RF ‘short circuited’ at one end is:

$X = R_c \tan(\beta l)$.

And, the volt-ampere product of such a line is:

$V^2\beta l/\{R_c \sin^2(\beta l)\}$

where:

V is the RMS value of the RF voltage at the end not ‘short-circuited’

βl is again the electrical line length in radians.

3.3.2 Choice of components

3.3.2.1 INDUCTORS

Depending on the value of the inductance required, inductors can be made in the form of a length of wire or a coil having one or more turns:

– straight wire

  The inductance of a straight wire is:

  $L = 0.46\ l \log (1.47\ l/d)$ nH.

  where l is the length of the wire and d the diameter, both in mm.

– single turn coil

  The inductance of a single turn of wire is:

  $L = 1.44D \log (1.08\ D/d)$ nH.

  where:

  D is the diameter (wire centre to wire centre) of the turn and d the wire diameter, both in mm.

– multi-turn coil

  The inductance of a coil with more than one turn wound in a single layer is:

  $L = n^2D^2/\{1.013\ (l + 0.45D)\}$ nH

  where:

  n is the number of turns

  D is the diameter (wire centre to wire centre) of the coil in mm

  l is the length of the winding in mm.

  The accuracy of the last formula is better than 1% provided $l > 0.45D$.

The formulae above indicate that the same inductance can be realized in different ways. An important point is the choice of the wire diameter. And, as a guideline, it is recommended to limit the current density to 2 to 3 A/mm^2. Although this guideline stems from the design of AF transformers and chokes where the windings are packed tightly together, it is relevant for inductances used at RF, as the series resistance due to skin-effect at high frequencies will be considerably greater.

Another point to consider for single layer coils is the ratio of the length of the winding to the diameter of the coil. The best ratio is 1 to 2 to get a high unloaded Q-factor. Providing some spacing between the turns will improve this Q-factor, and the recommenced spacing is equal to the wire diameter.

3.3.2.2 FIXED CAPACITORS

The most important properties of a capacitor for use in matching networks at high frequencies are:

– Maximum operating voltage

– Unloaded Q-factor

– Series inductance

– Size (in relation to dissipation)

– Temperature coefficient.

Nowadays, ceramic multilayer SMD capacitors (chip capacitors) are widely used, these having largely superseded leaded cylindrical and rectangular ceramic types. The Philips multilayer range contains Class 1, NPO types in different sizes and with maximum operating voltages up to 500 V (Ref.9). Class 1 means a relatively low ε_r and tan δ. NPO denotes a low temperature coefficient. Whilst these capacitors are suitable for many applications, a capacitor meeting more stringent specifications may be required in some applications.

The series inductance of most chip capacitors is about 1 nH. The VA-product that a chip can handle can be estimated as follows. Suppose a (small) chip can dissipate 300 mW and the unloaded Q-factor is 300, then the VA-product is the product of these two quantities:

$VI = 0.3 \times 300 = 90$ VA

If a specific application requires a higher VA-product, a parallel and/or series combination of chips can be used.

3.3.2.3 TRIMMERS

For VHF and UHF circuits, there are some excellent trimmers with Teflon isolation in Philips' product program (e.g. the 809 series, Ref.9). These have maximum operating voltages of 200 to 300 V, a maximum operating temperature of 125 °C and a guaranteed unloaded Q-factor between 400 and 670 at 100 MHz. They can be used up to about 1 GHz (their series inductance is 5 to 8 nH). At higher frequencies, products such as 'Gigahertz Trimmer Capacitors' from Tekelec (Johansson) are suitable. These have a self-resonant frequency well above the frequency of operation.

The power handling of these trimmers is much higher than that of chip capacitors. Some reserve is desirable because of the higher series inductance of trimmers. Parallel connection with chip capacitors is recommended to optimize the size of the control range.

3.4 Amplifier configurations

Most RF power amplifiers are ‘single-ended’, i.e. they have one power transistor. Sometimes, however, there are good reasons for using amplifiers having two or more transistors, as for example described in Section 3.2.2.5.2. In such cases, there are several ways to interconnect the transistors, the most popular employing:

– Hybrid couplers (90° phase difference)
– Parallel connection (0° phase difference), or
– Push-pull or balanced connection (180° phase difference).

3.4.1 Hybrid couplers

The use of hybrid couplers has already been described in the wider discussion of input networks in Section 3.2.2.5.2 just referred to. There, two single-ended stages were combined using 3 dB, 90° hybrid couplers to provide impedance matching *and* a flat power gain over a wide band of frequencies. The reader is referred back to that section for further details.

3.4.2 Parallel connection

3.4.2.1 VHF AND UHF RANGES

Sometimes, in base stations for mobile radio, output powers higher than those that can be delivered by a single transistor are required. The simplest solution is then to connect two transistors in parallel. However, because the transistor impedances can be very low, it is not recommended that this be done directly (i.e. by connecting gate-to-gate and drain-to-drain). A better method is shown in Fig.3-48.

Adjacent the transistors, separate matching sections are used; elsewhere, the sections are common to both transistors.

Resistors R_1 and R_2 are included to prevent push-pull oscillations, and perform the function of a hybrid coupler. Although this circuit does not fully isolate the transistors, it does prevent oscillations. For the best performance, R_1 should be twice the equivalent parallel input resistance and R_2 twice the load resistance of one transistor.

In Fig.3-48, only the RF components are shown. DC components such as RF chokes, coupling and decoupling capacitors still have to be added.

3.4.2.2 HF RANGE

Another form of parallel connection is often used in high-power amplifiers for the HF range. An extensive description of such a system is given in application report *“AN98032”*. The combining transformer (transmission line type) used is also described in report number *“ECO6907”*.

3.4.3 Push-pull (balanced) connection

To obtain more power than that obtainable from a single transistor, two transistors can be operated in push-pull mode (i.e. with 180° phase difference). To assist designers, several dual transistors already configured for push-pull are available from Philips. MOS and bipolar types for VHF and UHF operation are available.

The main advantage of push-pull is the good suppression of even-order harmonics and intermodulation products, simplifying the design of harmonic filters. It is therefore used extensively in HF SSB transmitters, as well as in FM broadcast and TV bands III, IV and V.

In the HF range, baluns (balanced to unbalanced transformers) can usually be combined with the required impedance transformation. This is done with transmission line or conventional transformers with ferrite cores as described in application reports *“ECO6907”* and *“ECO7213”*.

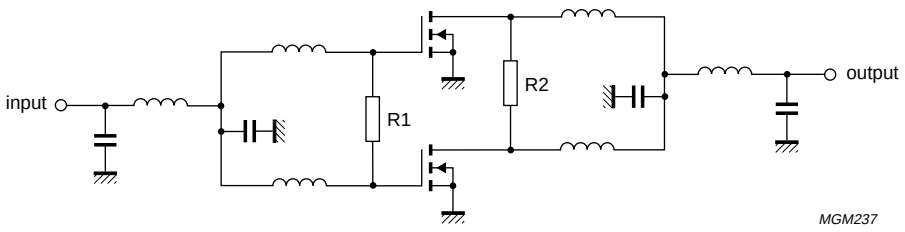


Fig.3-48 Two-transistor power amplifer with matching sections. This arrangement is also suitable for bipolar transistors.

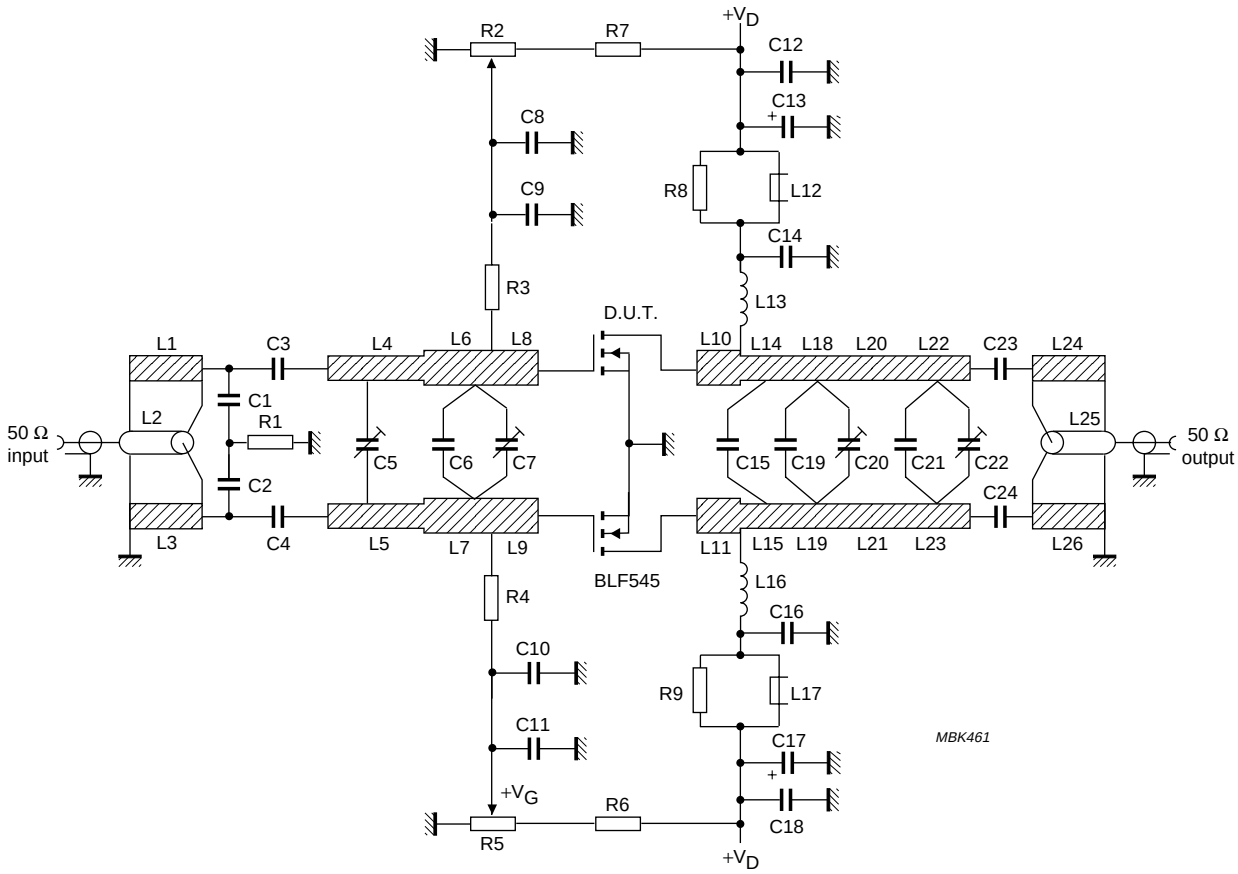


Fig.3-49 BLF545 test circuit. Full details of components are given in the BLF545 data sheet.

In the VHF and UHF ranges, another kind of balun is often used. Take, for example, the 500 MHz test circuit of the BLF545 (Fig.3-49). Although this is a narrow-band circuit, the balun used is a wideband type with a bandwidth of approximately one octave. Note that owing to the operating frequency, extensive use is made of striplines.

The baluns are both at the input (L_1, L_2 and L_3) and at the output (L_{24}, L_{25} and L_{26}). The input balun splits the signal on a 50 Ω basis (asymmetrical) into two signals in antiphase, each of half the input power. At the output, the reverse takes place.

A very convenient way of realizing this is by means of a semi-rigid coax cable with a characteristic resistance of 50 Ω. Looking at the output balun in Fig.3-49, we see that this is L_{25} and that its outer conductor is grounded at the output side while at the input side of this cable, both the inner and outer conductors are floating.

The best isolation will be obtained if the cable length (inner and outer conductors) is 1/4 λ for the centre of the frequency band (500 MHz). A disadvantage however is the impractical length of the cable.

A better solution is to use a cable length of about 1/8 λ soldered on top of a print track of the same length. The track width must of course be somewhat larger than the cable diameter so the two can be soldered together.

The signal that reaches the outer conductor of the cable via C_{24} is now shunted by a short stripline with an R_c of about 48 Ω and 1/8 λ long. The reactance of this stripline is then:

$X_p = R_c \tan \beta l = 48 \tan 45° = 48\ \Omega$

To restore the symmetry, we have to shunt the other signal, reaching the inner conductor of the cable via C_{23} with a stripline of the same dimensions, as shown in Fig.3-50.

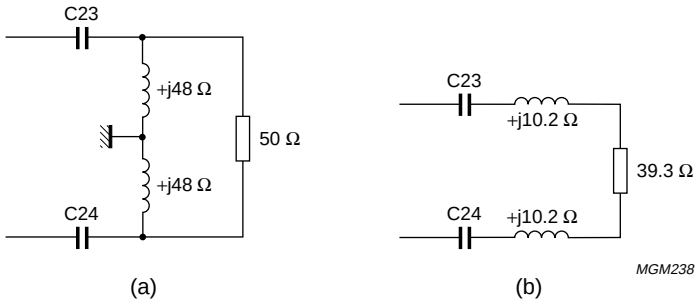


Fig.3-50 (a) Modified output baluns using 1/8 λ stripline; (b) Transformed circuit of (a) using the parallel-to-series transformation described in Section 3.2.1.1.

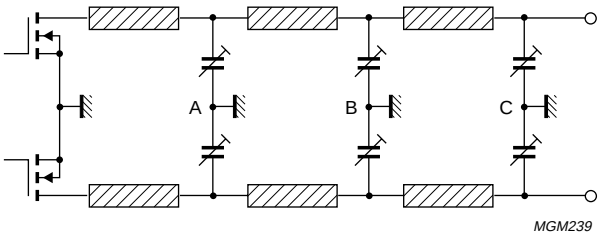


Fig.3-51 Output matching of a push-pull amplifier.

The last step is to choose the reactances of the capacitors C_{23} and C_{24} which have to be equal to the series-equivalent inductive reactances.

The result is that we have transformed the asymmetrical load resistance of 50 Ω to a symmetrical and real load resistance with a somewhat lower value. The latter is not a real problem as in many cases the transistor load impedance is lower still, so the balun forms part of the matching network.

In principle, the matching can be made for each section of the push-pull transistor separately as in Fig.3-51. However, it is not necessary to ground points A, B and C, so two capacitors in series can then be replaced by one of half the value, simplifying the circuit.

If the transistor operates in push-pull mode, it sees at its input the correct source impedance and at its output the correct load impedance. When analysing such a circuit in the parallel mode, it appears that in most cases the abovementioned conditions are not met at all. Both the input and the output circuits are practically unloaded so a parallel mode of oscillation (as opposed to the normal push-pull oscillation) can easily occur at a frequency far below the operating frequency. A good remedy is to introduce damping at the input and/or the output for this parallel mode which has no influence on the push-pull operation. An example is the combination C_1-C_2-R_1 in the BLF545 test circuit (Fig.3-49).

Another possibility is to shift the resonant frequency in the parallel mode by a large amount. This can be done for example at the input by not soldering the coax cable L_2 on L_1 but by loading it with a ferrite tube or several beads.

L_2 can also be wound on a ferrite toroid. The tracks L_1 and L_3 then become superfluous and the values of capacitors C_3 and C_4 must be increased as they now have only the function of coupling capacitors. Suitable grades of

ferrite are 4B and 4C. If a toroid is used, the inductance of the outer conductor of L_2 will be increased considerably. And although this inductance has a relatively large loss factor in the VHF/UHF range, if the impedance is high enough then the gain loss is rather small. An example of this method can be found in the 108 MHz test circuit of the BLF278 (see *"Data Handbook SC19a"*).

Returning to the BLF545 circuit at 500 MHz, we see the input balun compensated differently to the output one. L_1 and L_3 are tuned by the parallel capacitors C_1 and C_2, so there will be no transformation of the source resistance.

A good example of a wideband push-pull power amplifier using the baluns described above can be found in Application note *"AN98014"*. This amplifier delivers 150 W in TV-band IV/V and uses a BLV862 transistor.

3.5 Miscellaneous

3.5.1 Alignment of RF power amplifiers

In most cases, test circuits are aligned for maximum power gain and minimum input reflection. Sometimes a situation of very high power gain and moderate efficiency arises. This indicates that the circuit is very close to instability. Often, this is because the output network has been aligned in such a way that the transistor is loaded inductively, introducing (via the feedback capacitance) a negative resistance component at the input.

Though extra damping at the input lowers the gain and improves stability, it often does not raise efficiency. In such cases, it is better to align the output network with a dummy load. This procedure is also recommended for linear amplifiers such as those in SSB transmitters and in TV transposers and transmitters where the main aim is to minimize distortion. A dummy load for a 4-lead transistor with a stud or flange envelope can be made using a small piece of printed-circuit board as shown in Fig.3-52.

Between the collector and emitter connections of a bipolar transistor (or between the drain and source connections of a MOS transistor), an SMD resistor and an SMD multilayer capacitor of the correct value are connected in parallel. Together, these components form the complex conjugate value of the optimum load impedance of the transistor. Note, the values of resistor and capacitor for the dummy load can be determined using the guidelines given in Section 3.2.2.5.1.

The dummy load is placed in the circuit instead of the transistor. At the 50 Ω output, a signal generator is connected via a directional coupler to measure the reflection coefficient.

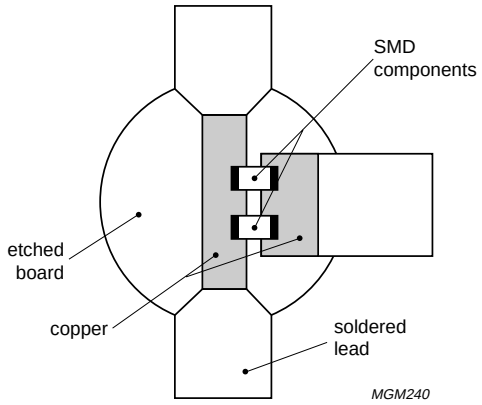


Fig.3-52 Dummy load made using printed-circuit board and SMD components. Though the dimensions are not critical, it is convenient to mimic those of a transistor to form a drop-in transistor replacement during alignment.

The output network is adjusted for zero reflection. After this procedure the network, loaded with 50 Ω, will provide the correct load impedance to the transistor and further alignment is not advised.

For push-pull transistors, the same method can be followed, but with two identical loads on one piece of printed-circuit board.

For wideband amplifiers too, this method is highly recommended. The signal generator has to be of the swept-frequency type, e.g. an R & S Polyskop or HP network analyzer.

For input networks of wideband amplifiers (see Fig.3-53) another method must be followed.

In this amplifier, capacitors C_1 and C_4 are partly variable (they are the parallel connection of a chip capacitor and a trimmer), while C_2 and C_3 are fixed (chip capacitors). The inductances L_2 and L_3 are relatively small and are therefore executed as striplines.

When aligning the output network by means of a dummy load, C_4 can first be varied to get the reflection over the whole frequency band within the required limits. If this is not sufficiently successful, C_3 can be varied in steps until the desired result is obtained. In most cases the results are then satisfactory; sometimes, L_4 must also be involved in this process.

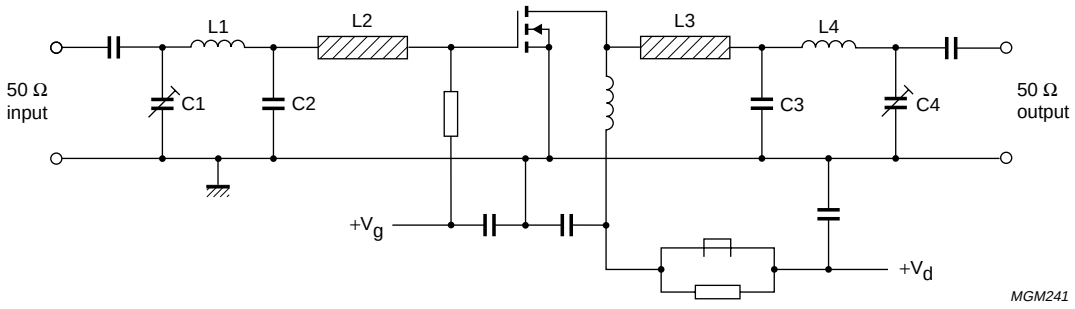


Fig.3-53 Typical wideband amplifier.

To align the input network, the transistor is put into the circuit, the 50 Ω load resistance is connected and the normal supply voltage applied. The bias voltage is adjusted in such a way that the transistor operates in class-A with a dissipation close to the desired output power, see data sheet for suitable values. Subsequently, the input network is aligned for minimum reflection over the desired frequency band. Compared with the output network this must be done in reverse order, namely C_1 first and when this is not sufficient also C_2, and in the last resort L_1.

This class-A alignment of the input network, done with small input signals, brings us very close to the final result. The last fine tuning of this network can then take place in the intended class of operation and with normal bias and RF drive powers for the required output power.

3.5.2 Suppression of parasitic oscillations

Oscillations at or near the frequency of operation can occur both with bipolar and MOS transistors especially in the lower VHF region. A suitable damping resistor between base and emitter (or between gate and source) will stop this type of oscillation.

Another type of oscillation occurs mainly with bipolar transistors although under certain circumstances with MOS devices too. This oscillation has to do with the biasing method. The collector or drain RF choke has a much higher inductance than the tuning elements and together with the total capacitance from collector or drain to earth it forms a resonant circuit at a frequency far below the operating one.

Sometimes a similar situation exists at the input side especially with bipolar transistors. If these circuits are not well damped, parasitic oscillation at relatively low frequency can start due to the always present feedback capacitance.

The best remedy is a combination of components giving strong damping at low frequencies and very little damping at the frequency of operation. Generally speaking, transistors should be loaded at both their input and output with a low, mainly resistive impedance. This can be provided at the input side with the circuit of Fig.3-54(a) and at the output side with the circuit of Fig.3-54(b) or (c).

In all these circuits, L_1 is a relatively small inductance with a high Q-factor and a reactance at the operating frequency of 3 to 7 times the equivalent parallel resistance at that point. L_2 is a much higher inductance with a low Q-factor, e.g. a choke with a ferrite core (3B being a good material). The inductance can be 6 to 8 μH.

R is a small resistor, say 10 Ω. C1 is a decoupling capacitor for the operating frequency, i.e. a low value ceramic type with high Q-factor. C_2 is a much higher capacitance, e.g. 100 nF which can have a low Q-factor.

Sometimes the supply voltage is decoupled with an extra capacitor which can be a low value electrolytic type (not drawn).

Another form of parasitic oscillation is parametric oscillation caused by the non-linear-properties of the collector capacitance. If this capacitor is fully driven by the RF voltage, it can develop a negative resistance at one half and even one third of the RF frequency, leading to instability when the collector or drain RF choke has a very low value.

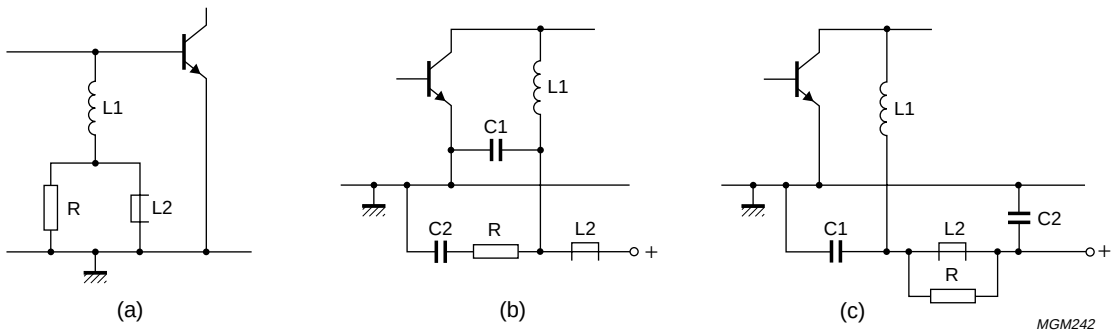


Fig.3-54 Circuit parts to suppress parasitic oscillations (a) at the input; (b) and (c) at the output.

Also possible is a parametric oscillation known as conversion oscillation. This can happen when the collector or drain circuit contains two resonant circuits where the sum of the resonant frequencies equals the frequency of operation. The lower one is then formed by the RF choke and the total effective parallel capacitance while the other is the slightly detuned output matching circuit.
This detuning can arise during tuning or by a small antenna mismatch.

Mathematically it can be shown that the power of this oscillation is divided into the ratio of the resonant frequencies of the tuned circuits. Fortunately, the measures necessary to stop this oscillation are the same as those previously mentioned.

4 RF AND MICROWAVE TRANSISTOR PACKAGES

The packages of electronic devices are, in general, designed to:

– Protect the electronics from mechanical damage

– Ensure adequate heat transfer to the ambient, and

– Provide robust, solderable electrical terminations.

For RF and microwave transistors however, the package itself forms an important part of the total electronic circuit, and this places additional requirements upon its electrical characteristics.

These requirements together with the available technologies have influenced RF transistor package design over the years. As a result, there are a variety of packages on the market today. The design and characteristics of the main package types are outlined in the following sections. Information on specific packages is given in data handbooks SC18: Discrete Semiconductor Packages, and SC19a: RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators.

4.1 Basics of RF and microwave transistor packages

In general, two (the base/gate and emitter/source) of the three electrical contacts of a transistor die are on the top of the die, and are connected to the external package terminations by bonding wires. The underside of the die is the third contact (the collector/drain) and connection is usually made to this contact by bonding the die to an electrical conductor which also serves as a heatsink.

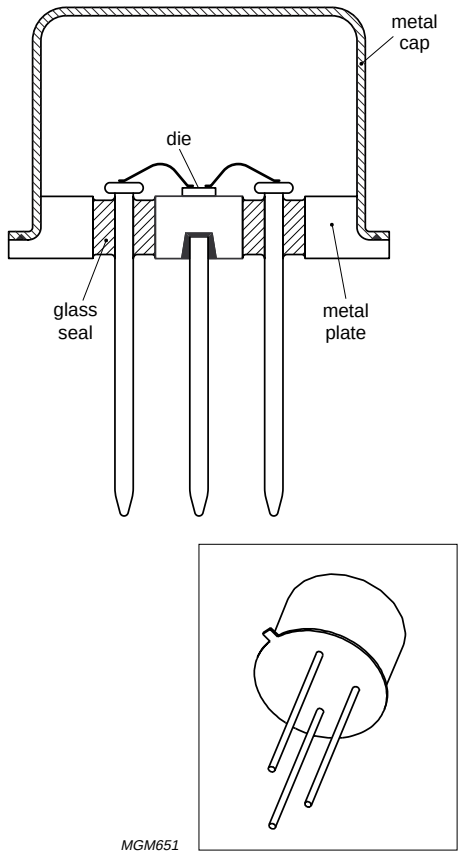


Fig.4-1 Metal-can package construction.

4.2 Metal-can packages

Included here for historical completeness, metal-can packages used to house bipolar transistors are rapidly being replaced by newer, superior alternatives.

In a metal-can package (e.g. TO-39 (SOT5)), the transistor die is attached to a small, thin metal plate (usually round). All the external electrical terminations are wire leads. The collector lead is connected to the plate; the emitter and base leads are fed through the plate and isolated from it by a glass seal.

The package is sealed with a metal cap welded onto the plate. This design combined with stringent well-controlled manufacture provide a hermetic package.

The power that a metal-can package can handle however is very limited, because heat is mainly removed from the die by radiation. And, while mounting the package directly onto a heatsink in a circuit lowers the packages thermal resistance, it means the collector is connected to the heatsink, whereas most applications require a common-emitter or common-base configuration. The solution to this drawback was found with the introduction of ceramic packages.

4.3 Ceramic packages with a copper stud or flange

In a ceramic package, the transistor die is soldered on a metallized ceramic heat-spreader located on top of a stud or flange used to mount the transistor and to conduct heat away from the die. The function of the somewhat inappropriately named heat-spreader is to electrically isolate the bottom of the die from the stud or flange, allowing the transistor package to be mounted directly to a heatsink.

The electrical terminations are formed by brazing several, usually flat, leads to the heat-spreader, with wire bonding from the leads to the two contacts on top of the die. Beryllia (BeO) used to be the most-commonly used heat-spreader

material since it combines good thermal conductivity (250 W/mK) with good electrical isolation. A disadvantage of BeO is that it is toxic. So, in line with Philips' policy to eliminate toxic and environmentally harmful substances from its products, packages with aluminiumnitride (AIN) heat-spreaders have been developed - the slightly lower thermal conductivity of AIN being compensated for by using thinner ceramic.

The first ceramic packages incorporated a copper stud or flange brazed to the bottom of the heat-spreader. Since there is considerable mismatch between the thermal coefficients of expansion (TCE) of copper and beryllia, the contact area must be limited to prevent the heat-spreader from cracking. Larger (higher power) packages (e.g. SOT121 and SOT171) were therefore designed using a copper pedestal to which the heat-spreader was attached (brazed) with the die on top. The pedestal allows a larger heat-spreader (and hence die) to be used whilst maintaining the metal-to-ceramic contact area well below the practical limit. Even with this design, however, the size of the heat-spreader is limited as only the region directly above the pedestal has a low thermal resistance, and thus conducts heat effectively. Those areas of a transistor die and heat-spreader extending beyond the top of the pedestal have a higher thermal resistance. Nevertheless, since such packages can be mounted directly onto a heatsink in the application, the power handling, though still restricted, is much better than that of the standard design.

This type of package (with or without pedestal) is sealed by epoxy-glueing a ceramic cap to the top of the package. Though forming a high-quality reliable seal, epoxy resin does not provide a hermetic barrier. To ensure that the package is completely sealed and that there are no pinholes in the epoxy, the packages are tested for gross leaks. Note that all epoxy glues start to degrade at temperatures close to 300 °C and, for long-term stability, standard ceramic packages should not be exposed to temperatures above about 150 °C. Short exposure to higher temperatures is allowed (e.g. during reflow soldering). In addition, during fluxing and cleaning, minimize exposure to liquids, for example by dipping.

Though not strictly hermetic, all of Philips' standard ceramic packages contain glass-passivated transistor dies. Effectively isolating the die from its surroundings, glass passivation contributes to extremely high levels of transistor reliability.

4.4 Ceramic packages with special flange materials

As indicated above, the size of ceramic packages with copper flanges is limited by the different TCEs of copper and ceramic. This limitation was overcome by replacing the copper by a material with a much lower TCE. Nowadays, two materials are commonly used which combine a much lower TCE with a still acceptable thermal conductance:

– A tungsten-copper alloy (e.g. SOT262), and
– A copper-molybdenum-copper sandwich (e.g. SOT468).

These materials allow the contact area between flange and ceramic to be much larger while the ceramic can be even thinner without increased risk of cracking. Since these materials are at present very expensive, packages with a copper flange remain in widespread use. For improved RF grounding at high frequencies, flanged packages with through-plated holes in the ceramic have been developed.

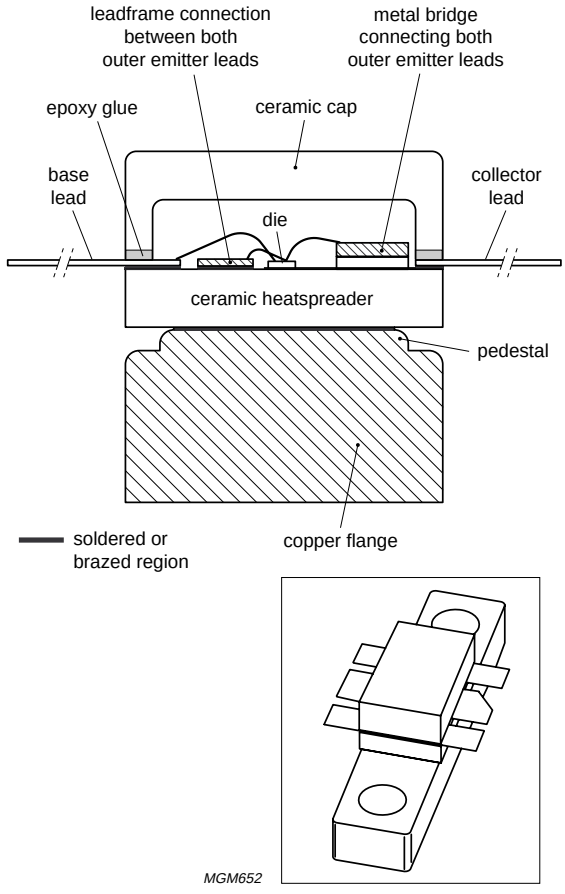


Fig.4-2 Construction of a typical ceramic package with flange.

4.5 Hermetic ceramic packages

A hermetic transistor package provides the highest levels of reliability in extremely harsh environments as required in aerospace and military applications for example.

Ceramic packages can be made hermetic, however a special design is required. The leads are no longer brazed directly onto the heat-spreader as in a standard ceramic package but are brazed onto a two-layer alumina frame (i.e. consisting of two frames sintered together). The bottom frame is larger than the top one, thus forming inner and outer ledges (electrically connected by metallization on the bottom frame) The external leads are brazed to the outer ledge, while the inner ledge is used to make a connection to the transistor die by wire-bonding. The top side of the second frame is flat and completely metallized to enable a metal or ceramic cap to be soldered to it.

4.6 LDMOST packages

Whereas the abovementioned packages are suitable for bipolar and VDMOS transistors, packages for the LDMOS transistors are somewhat different. This is because the bottom of an LDMOST die is the source, not the drain (collector) as in a standard MOS (bipolar) transistor. This is a major advantage as it is no longer necessary to electrically isolate the die from the heatsink in the application - the die is mounted directly on the flange. The flange material therefore must have a good thermal conductivity and a TCE close to that of silicon. Two materials in current use are a tungsten-copper alloy flange, and the copper-molybdenum-copper sandwich mentioned earlier. In order to electrically isolate the drain and gate leads from the flange, an alumina frame is brazed onto the flange, with the leads brazed on top of this frame. The package is completed by a ceramic cap sealed with epoxy.

Offering superb electrical and thermal performance, and ease of heatsinking, Philips' LDMOS packages are an attractive solution in an increasing number of applications.

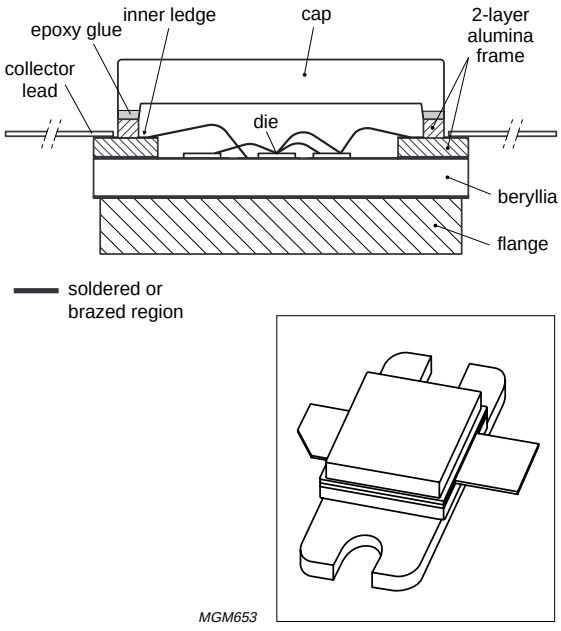


Fig.4-3 Typical hermetic package construction (Package: SOT422A).

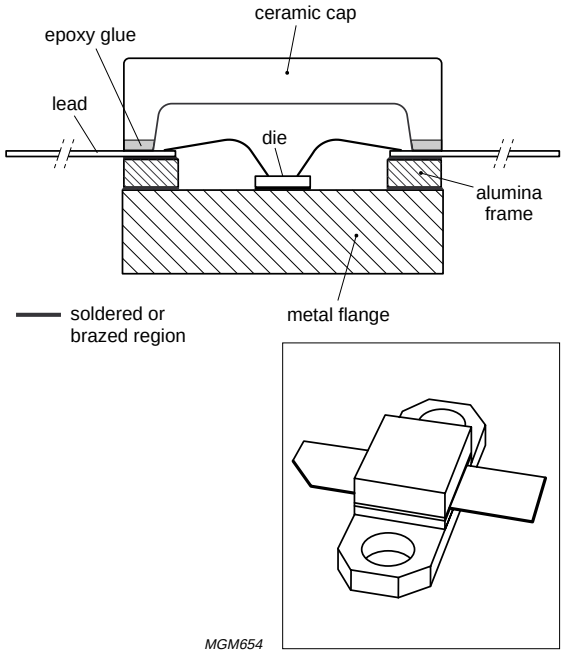


Fig.4-4 Typical LDMOST package construction (Package: SOT467).

4.7 Flangeless and SMD packages

In order to reduce the board space required by transistors, packages without a flange have been introduced (e.g. SOT333). Eliminating the flange however also eliminates the mounting holes, so other mounting methods have to be used. These include clamping or even reflow soldering. Eliminating the flange is in general only possible with packages for bipolar devices in which the dies are mounted on a ceramic heat-spreader. However, for Philips' SOT391B package, eliminating the flange alone was not an option as this package has through-plated holes in the heat-spreader. Without a flange, the package could not be sealed adequately. The solution is to braze a thin copper plate to the back of the package. This has two advantages. First, the holes are sealed, and second, the lead height of the package can be optimized to suit standard printed board materials.

With LDMOST packages, the entire flange cannot be eliminated as the dies are mounted on top of the flange. The board space required can be reduced however by reducing the length of the flange, most effectively by shortening it to the size of the alumina frame. Packages with such modified flanges are often referred to as 'earless'. Clamping or reflow soldering are again the recommended mounting methods.

Besides flangeless and earless packages, Philips has introduced a leaded surface-mount package (SOT409). This package, which is based upon the plastic SO8 package, has a copper backpad, a ceramic (alumina or AIN) heat-spreader, a copper leadframe extending beyond the heat-spreader and a ceramic cap. The backpad enables the package to be soldered onto a PCB. To ensure reliable solder joints and low thermal resistance, the specification stipulates that the leads are J-shaped such that backpads and leads are coplanar to within 0.1 mm, and that the leads never extend beyond the backpad plane.

An even more effective way of reducing the required board area is to use leadless packages. Besides saving board space, these are highly cost-effective as they can be mounted in a standard automated SMD reflow soldering process. This kind of package consists of a ceramic (AIN) heat-spreader and a ceramic cap. Leads are replaced by plated contacts on the package sides. To increase the soldering area for the electrical connections (and to obtain more reliable solder joints), the plating is extended onto the back of the package.

Reflow soldering footprints are available for all SMD packages for optimum soldering results. For optimum heat flow between package and heatsink (through a printed circuit board), it is recommended to incorporate vias in the board. The optimum size and location of these vias for each package are available.

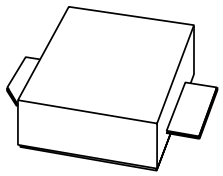


Fig.4-5 SOT391B - a typical flangeless ceramic package.

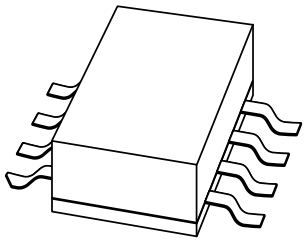
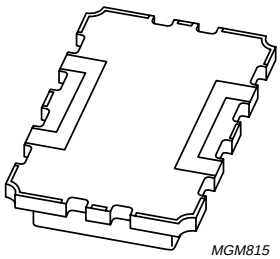


Fig.4-6 SOT409B - a ceramic surface-mount transistor package derived from the SO8 package.



Bottom view

Fig.4-7 SOT511 - a typical leadless ceramic surface-mount package.

4.8 Coefficients of linear thermal expansion of packages

The data of Tables 4-1 and 4-2 (together with manufacturers' board and heatsink data) can be used to obtain good thermal matching in practical amplifiers.

Table 4-1 Overview of materials used in packages

PACKAGE	FLANGE			LEADFRAME				BACKPAD	CERAMIC INSULATOR	
	COPPER	TUNGSTEN -COPPER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29)	COPPER	COPPER	BeO	AIN
SOT119	√	–	–	√	–	–	–	–	√	–
SOT121	√	–	–	√	–	–	–	–	√	–
SOT123	√	–	–	√	–	–	–	–	√	–
SOT161	√	–	–	√	–	–	–	–	√	–
SOT171	√	–	–	√	–	–	–	–	√	–
SOT262	–	√	–	√	–	–	–	–	√	–
SOT268	–	√	–	√	–	–	–	–	√	–
SOT273	√	–	–	√	–	–	–	–	√	–
SOT279	√	–	–	√	–	–	–	–	√	–
SOT289	–	√	–		–	√	–	–	√	–
SOT324	–	√	–	√	–	–	–	–	√	–
SOT333	√	–	–	√	–	–	–	–	√	–
SOT390	–	√	–	√	–	–	–	–	√	–
SOT391	–	√	–	√	–	–	–	–	√	–
SOT391B	–	–	–	√	–	–	–	√	√	–
SOT409	–	–	–	–	–	–	√	√	–	√
SOT422	√	–	–	–	√	–	–	–	√	–
SOT423	√	–	–	–	√	–	–	–	√	–
SOT437	–	√	–	√		–	–	–	√	–
SOT439	√	–	–	–	√	–	–	–	√	–
SOT440	√	–	–	–	–	√	–	–	√	–
SOT443	–	√	–	–	–	√	–	–	√	–
SOT445	√	–	–	–	–	√	–	–	√	–
SOT448	–	√	–	–	√	–	–	–	√	–
SOT460	–	√	–	√	–	–	–	–	√	–
SOT467	–	√	–	√	–	–	–	–	–	–
SOT468	–	–	√	√	–	–	–	–	–	√
SOT502	–	√	–	√	–	–	–	–	–	–
SOT511	–	–	–	–	–	–	–	–	–	√

Source: Suppliers' data sheets

Table 4-2 Coefficients of linear thermal expansion, α, (in ppm/K) of package materials between 25 and 150 °C;

COPPER	TUNGSTEN COPPER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29/Co17)	BERYLLIA	ALUMINIUM NITRIDE
17.9	6.6	9.5-6.0	4.5	11.6	4.4	6.7	4.0

Source: Suppliers' data sheets

4.9 Mounting recommendations

When mounting transistors, observing the following recommendations will ensure good thermal and good electrical contact between transistor package and heatsink - a requisite for trouble-free, reliable operation.

4.9.1 Heatsink preparation

– For transistors dissipating up to 80 W, heatsink thickness should be:
  - At least 3 mm for copper heatsinks (>99.9% ETP-Cu)
  - At least 5 mm for aluminium heatsinks (99% Al)

  These thicknesses should be increased proportionally for transistors dissipating more power.
– Minimum depth of tapped holes in heatsinks: 6 mm
– Ensure holes in heatsinks are free of burrs
– Ensure that the mounting area is at a level such that there is a small positive clearance between the transistor leads and the printed circuit board. This prevents any upward bending of the leads which can damage the ceramic heat-spreader and/or the encapsulation.
– Flatness of the mounting area: better than 0.02 mm
– Mounting area roughness: <0.5 μm
– Mounting area should be free of oxidation.

4.9.2 Printed circuit board preparation

– Tin and wash the printed circuit board.

4.9.3 Transistor preparation

– Transistor leads are gold plated. To avoid brittle solder joints (due to too much gold in the joint), pre-tin the leads, for example, by dipping their full length into a solder bath at a temperature of about 230 °C. Minimize the use of flux.
– Apply a thin, evenly-distributed layer of heatsink compound to the flange
– Recommended heatsink compounds are:
  - 'WPS II' (silicone free) Austerlitz-Electronics
  - '340' from Dow Corning.
– When using a thermal pad, take special care with respect to the size as well as the positioning of the pad. If the pad does not cover the entire flange, the package can be stressed so much that the ceramic heat-spreader cracks. Ensure that mounting screws do not contact the thermal pad (prevents the pad wrinkling if the screws are turned).

4.9.4 Mounting sequence

– Position the device with the washers in place
– Use 4-40 UNC-2A cheese-head screws with a flat washer to spread the joint pressure
– Tighten the screws until finger tight (0.05 Nm)
– Further tighten the screws until the specified torque is reached (do not lubricate); for torques, refer to the package outlines section of each data handbook
– To lock mounting screws, allow about 30 minutes for them to bed-down after the specified torque has been applied, re-tighten to the specified torque and apply locking paint
– Solder the transistor leads onto the printed circuit board.

5 SYMBOLS

Table 5-1

α	Coefficient of linear thermal expansion
βl	Electrical line length (stripline)
γ	Mathematical variable
ε_r	Dielectric constant (relative)
ε	Mathematical variable
η_c	Collector efficiency
λ	Failure rate; wavelength
ω	Angular frequency; maximum angular frequency; minimum angular frequency
ω_T	Transition frequency ($2\pi f_T$)
A	Attenuation; difference in IMD between driver and final stage
B	Susceptance; absolute bandwidth; increase in IMD in amplifier output
C	Capacitance
C_c	Total collector or output capacitance
C_{re}	Feedback capacitance, i.e. C_{cb}
C_{is}	Input capacitance when the output is short-circuited
C_{os}	Output capacitance when the input is short-circuited
C_{rs}	Feedback capacitance; this is the same as C_{gd}
C_p	Parallel capacitance
C_s	Series capacitance
d	Intermodulation distortion; mathematical variable
$E_{(SBR)}$	(Reverse) second breakdown energy
f	Frequency
f_T	Transition frequency
G	(Power) gain
g	(Normalized) filter element identifier (resistance, capacitance or inductance)
g_{fs}	Forward transconductance
h_{FE}	DC current gain
h_{fe}	RF current gain
I_C	Collector DC current (i_c denotes varying value)
I_{CM}	Maximum instantaneous value of the collector current
I_D	Drain current
I_{DSX}	Maximum drain current that a device can deliver
k	Constant; mathematical variable: $k = \gamma + \sqrt{(\gamma^2 + 1)}$
L	Inductance
L_p	Parallel inductance
L_s	Series inductance
l_{ch}	Channel length
ppm	Parts per million
P_L	Load power
P_S	Forward power delivered by source
P_{tot}	Maximum RF dissipation at a mounting base temperature of 25 °C
R	Resistance
$R_{DS(on)}$	Total resistance in the drain-source circuit at a high, positive V_{GS}
R_h	Higher resistance
R_l	Lower resistance
R_L	Load resistance
R_p	Parallel resistance
R_s	Series resistance
r	Reflection coefficient
s	Voltage standing wave ratio
SOAR	Safe Operating ARea
T_{stg}	Maximum ($T_{stg\ max}$) and minimum ($T_{stg\ min}$) temperatures at which a device may be stored when not in operation
T_j	Maximum junction temperature in operation
$V_{(BR)CBO}$	Collector-base breakdown voltage with open emitter
$V_{(BR)CEO}$	Collector-emitter breakdown voltage with open base
V_{CBO}	Maximum collector-base voltage with open emitter
V_{CEO}	Maximum collector-emitter voltage with open base
v_{ce}	Collector-emitter voltage (instantaneous value)
V_{CES}	Maximum collector-emitter voltage with a short circuit between base and emitter
$V_{CE\ sat}$	Collector-emitter saturation voltage
V_{CER}	Maximum collector-emitter voltage with a small resistor e.g. 10 Ω, between base and emitter
V_{DS}	Drain-source voltage
V_{EBO}	Maximum emitter-base voltage with open collector
V_{GS}	Gate-source voltage
$V_{GS(th)}$	Gate voltage at which drain current starts to flow
VSWR	Voltage standing wave ratio
X	Reactance
X_p	Parallel reactance
X_s	Series reactance

6 REFERENCES

6.1 References in the main text

1. Matthaei, G.L., Young, L., & Jones, E.M.T., 'Microwave filters, impedance-matching networks, and coupling structures', McGraw-Hill Book Company.
2. Matthaei, G.L., 'Tables of Chebyshev impedance transforming networks of the low-pass filter form'. Proc. IEEE, Aug. 1964, pp. 939-963.
3. Fleischmann, U., 'Breitband-anpassung mit 4 Reaktanzen unter Berücksichtigung des Übertragungsverhaltens', Nachrichten Elektronik, 1 - 1980, pp. 20-24.
4. Fleischmann, U., 'Transformierende Hoch- und Tiefpässe (I)', Nachrichten Elektronik, 35 - 1981, Heft 2, pp. 76-79.
5. Fleischmann, U., 'Transformierende Hoch- und Tiefpässe (II)', Nachrichten Elektronik, 35 - 1981, Heft 3, pp. 123-126.
6. Fano, R.M., 'Theoretical limitations on the broadband matching of arbitrary impedances', Journal of the Franklin Institute, Jan. 1950, pp. 57-83.
7. Fano, R.M., 'Theoretical limitations on the broadband matching of arbitrary impedances', Journal of the Franklin Institute, Feb. 1950, pp. 139-154.
8. Wheeler, H.A., 'Transmission line properties of a strip on a dielectric sheet on a plane', IEEE Trans. on Microwave Theory and Tech. Vol. MTT-25 (1977), No. 8, pp. 631-647.
9. 'Passive Components, Product Selection Guide 1998'. Philips Components. Ordering code: 9398 238 22011.

6.2 Additional references

1. Black, J.R., 'Electromigration failure modes in aluminium metallization for semiconductor devices', Proc. IEEE, Sept. 1969, pp. 1587-1594
2. Cohn, S.B., 'Direct-coupled-resonator filters', Proc. IRE, Feb. 1957, pp. 187-196.
3. Cohn, S.B., 'A class of broadband three-port TEM-mode hybrids', IEEE Trans. on Microwave Theory and Techniques, Feb. 1968, pp. 110-116
4. Hilberg, W., 'Einige grundsätzliche Betrachtungen zu Breitband-Übertragern', NTZ, 1966, Heft 9, pp. 527-538.
5. Kazimierczuk, M.K., & Tabisz, W.A., 'Class-C-E high-efficiency tuned power amplifier', IEEE Trans. on Circuits and Systems, March 1989, pp. 421-428
6. Knauer,R., 'Nichtlineare Verzerrungen in Hochfrequenzverstärkern', Siemens-Zeitschrift 42, 1968, Heft 3, pp. 201-209.
7. Levy, R., 'Explicit formulas for Chebyshev impedance-matching networks, filters and interstages', Proc. IEEE, June 1964, pp. 1099-1106.
8. Löber,G., 'Reaktanzfilter optimaler Anpassung bis zum Grad 5', Frequenz 24, (1970) 2, pp. 54-62.
9. Matthaei, G.L., 'Short-step Chebyshev impedance transformers', IEEE Trans. on Microwave Theory and Techniques, Aug. 1966, pp. 372-383.
10. Minasian, R.A., 'Power MOSFET dynamic large-signal model', IEE Proc., April 1981, pp. 73-79.
11. Nielinger, H., 'Optimale Dimensionierung von Breitbandanpassungsnetzwerken', NTZ Heft 2, 1968, pp. 88-91.
12. Pitzalis Jr., O., and Gilson, R.A., 'Tables of impedance matching networks which approximate prescribed attenuation versus frequency slopes', IEEE Trans. on Microwave Theory and Techniques, April 1971, pp. 381-386.
13. Pitzalis Jr., O., and Couse, T.P.M., 'Practical design information for broadband transmission line transformers', Proc. IEEE, April 1968, pp. 738-739.
14. Raab, F.H., 'Idealized operation of the class-E tuned power amplifier', IEEE Trans. on Circuits and Systems, Dec. 1977, pp. 725-735.
15. Ruf, K., 'Leistungsregelung und Leistungsbilanz transistorisierter Sendeverstärker', Nachrichten Elektronik 12, 1979, pp. 400-402.
16. Young, L., 'Tables for cascaded homogeneous quarter wave transformers', IRE Trans. on Microwave Theory and Techniques, April 1959, pp. 233-237.